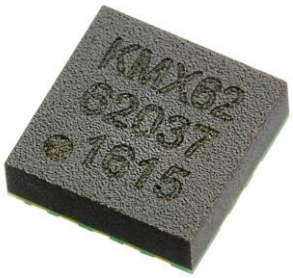
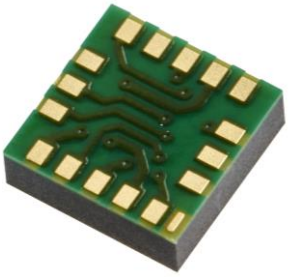
Kionix®	**Digital Tri-axis Magnetometer/ Tri-axis Accelerometer Specifications**	**PART NUMBER:** **KMX62-1031** **Rev. 3.0** **1-Mar-16**

Product Description





KMX62 is a 6 Degrees-of-Freedom inertial sensor system that features 16-bit digital outputs accessed through I^2C communication. The KMX62 sensor consists of a tri-axial magnetometer plus a tri-axial accelerometer coupled with an ASIC. It is packaged in a 3 x 3 x 0.9mm Land Grid Array (LGA) package. The ASIC is realized in standard 0.18um CMOS technology and features flexible user programmable ±2g/±4g/±8g/±16g full scale range for the accelerometer. Accelerometer and Magnetometer data can be accumulated in an internal 384 byte FIFO buffer and transmitted to the application processor.

Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. Capacitance changes are amplified and converted into digital signals which are processed by a dedicated digital signal processing unit. The digital signal processor applies filtering, bias and sensitivity adjustment, as well as temperature compensation.

Magnetic sensing is based on the principle of magnetic impedance. The magnetic sensor detects very small magnetic fields by passing an electric pulse through a special electron spin aligned amorphous wire. Due to the high Curie temperature of the wire, the sensor's thermal performance shows excellent stability.

Noise performance is excellent with bias stability over temperature. Bias errors resulting from assembly can be trimmed digitally by the user. These sensors can accept supply voltages between 1.7V and 3.6V, and digital communication voltages between 1.2 and 3.6V.

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Kionix®	**Digital Tri-axis Magnetometer/ Tri-axis Accelerometer Specifications**	**PART NUMBER:** **KMX62-1031** **Rev. 3.0** **1-Mar-16**

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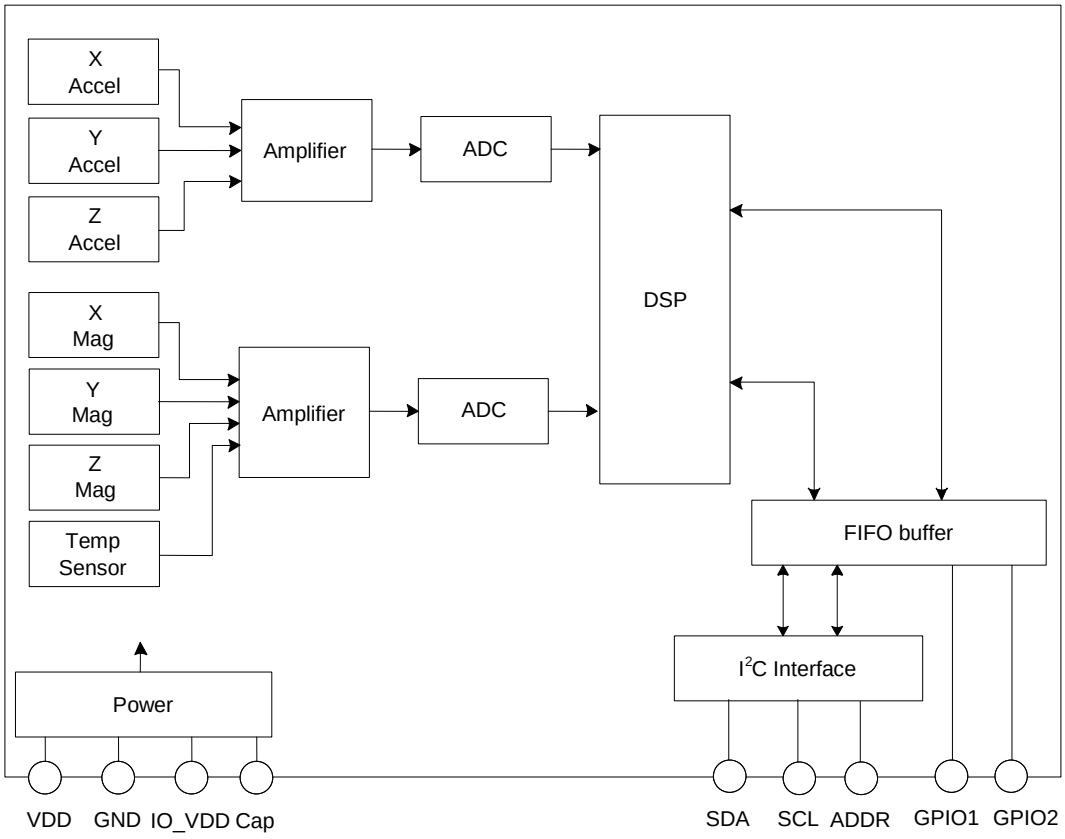
Functional Diagram



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Product Specifications

Note: Specifications are for operation at VDD = 2.5V and T = 25ºC (RES=1) unless stated otherwise

Magnetometer Specifications

Parameters	Units	Min	Typical	Max
Operating Temperature Range	ºC	-40	-	85
Full Scale Range	± µT		1200	
Digital Bit Depth	bits		16	
Offset at Zero Magnetic Field	± µT		0	
Offset Temperature Coefficient	± µT/ºC		0.3	
Magnetic Sensitivity	± µT/LSB		0.0366	
Sensitivity Accuracy	± %		20	
Sensitivity Temperature Coefficient.	± %/ºC		0.05	
Positive Self Test Output change on Activation	µT		800	
Negative Self Test Output change on Activation	µT		-800	
Integral Non-Linearity	% of FS		0.5	
Noise[1] (at 50Hz ODR)	µT (RMS)		0.3	
Cross Axis Sensitivity	% of FS		2.0 (XY) 0.5 (XZ) 0.3 (YX) 0.2 (YZ) 0.9 (ZX) 0.2 (ZY)	
Maximum Exposed Field[2]	µT			500,000

Table 1. Magnetometer Specifications

Notes:

1. See diagrams below for noise performance over ODR for all three axes.
2. No permanent effect on Zero Magnetic Field Offset.

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Accelerometer Specifications

Parameters		Units	Min	Typical	Max
Operating Temperature Range		ºC	-40	-	85
Full Scale Range	GSEL1=0, GSEL0=0	g		± 2	
	GSEL1=0, GSEL0=1			± 4	
	GSEL1=1, GSEL0=0			± 8	
	GSEL1=1, GSEL0=1			± 16	
Digital Bit Depth				16	
Zero-g Offset		mg		±25	±90
Zero-g Offset Temperature Coefficient		± mg/ºC		0.25	
Sensitivity	GSEL1=0, GSEL0=0 (± 2g)	mg/LSB		0.06	
	GSEL1=0, GSEL0=1 (± 4g)			0.12	
	GSEL1=1, GSEL0=0 (± 8g)			0.24	
	GSEL1=1, GSEL0=1 (± 16g)			0.49	
Sensitivity Accuracy		± %		5	
Sensitivity Temperature Coefficient		± %/ºC		0.01	
Positive Self Test Output change on Activation		g	0.25 (XY) 0.20 (Z)	0.5	0.75 (XYZ)
Sensor Mechanical Resonance (-3dB)[1]		Hz		3500 (xy) 1800 (z)	
Integral Non-Linearity		% of FS		1	
Cross Axis Sensitivity[2]		± %		-2.0 (XY) 0.1 (XZ) 2.7 (YX) -0.7 (YZ) -0.8 (ZX) 1.4 (ZY)	
Noise[3] (at 50Hz)		mg (RMS)		0.75	

Table 2. Accelerometer Specifications

Notes:

1. Resonance as defined by the dampened mechanical sensor.
2. As measured in a test socket. The cross axis sensitivity that is measured is the by-product of positional inaccuracies at all stages of test and assembly.
3. See diagrams below for noise performance over ODR for all three axes.

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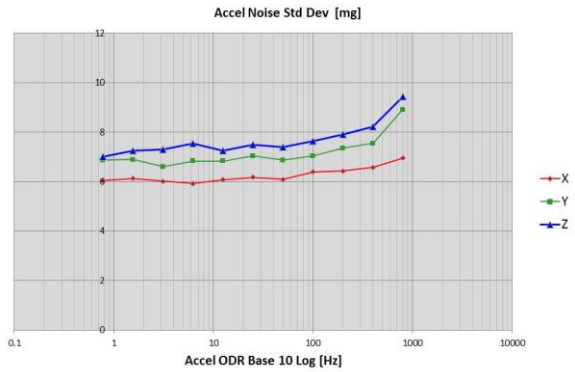
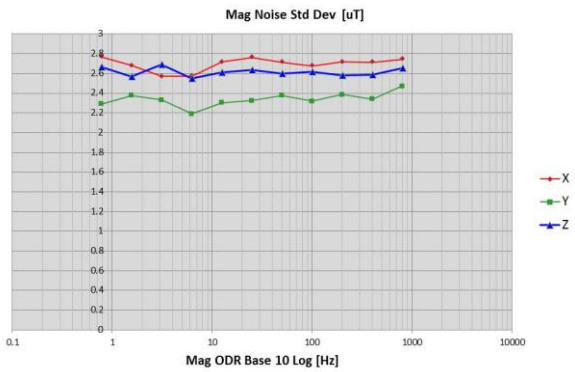
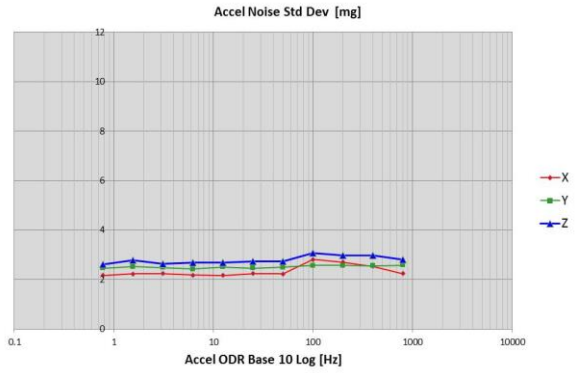
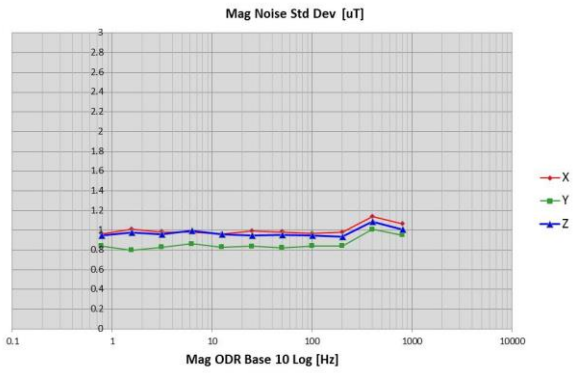
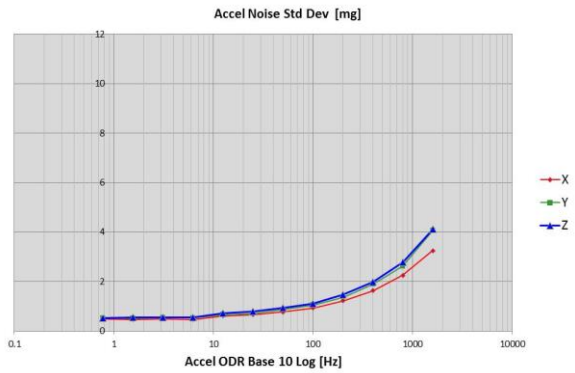
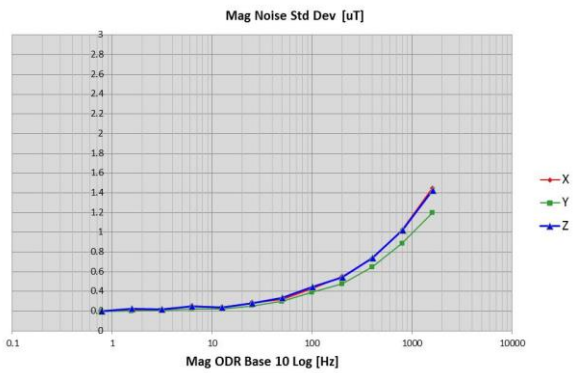
Noise Diagrams

Typical noise over selected ODR settings (0.781,1.563,3.125,6.25,12.5,25,50,100,200,400,800,1600Hz)

Res	Accel	Mag
00		
01		
10, 11		

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Temperature Sensor

(specifications are for operation at VDD = 2.5V and T = 25ºC unless stated otherwise)

Parameters	Units	Min	Typical	Max
Operating Temperature Range	ºC	-40	-	85
Output Accuracy	± ºC		5	
Sensitivity (16-bit digital)	counts/ ºC		0.0039	
Sensitivity (8-bit digital, TEMP<15:8>)	counts/ ºC		1	

Electrical Specifications

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Operating	V	1.7	2.5	3.6
I/O Pads Supply Voltage (IO_VDD)		V	1.2		3.6
Current Consumption[1] (High Resolution Mode) (<RES> = 10 or 11)	Operating (mag + accel)	µA		395	
	Magnetometer only			295	
	Accelerometer only			150	
	Standby			1	5
Output Low Voltage[2]		V	-	-	0.2 * IO_VDD
Output Low Voltage (IO_VDD > 2V)		V	-	-	0.4
Output High Voltage		V	0.9 * IO_VDD	-	-
Input Low Voltage		V	-	-	0.3 * IO_VDD
Input High Voltage		V	0.7 * IO_VDD	-	-
I²C Communication Rate[3,4]		MHz	0.1	0.4	3.4
Output Data Rate		Hz	0.781	100	25.6kHz
Filter -3dB Cutoff[5]	RES 00,01	Hz		800	
	RES 10,11	Hz		ODR/2	
Internal Oscillator Tolerance		%	-10		10
Start Up Time[6]		ms			

Table 3. Electrical Specifications

Notes:

1. See Current Consumption diagrams below for other modes (RES = 00 or 01).
2. Assuming I²C communication and minimum 1.5kΩ pull-up resistor on SCL and SDA.
3. Assuming max bus capacitance load of 20pF.
4. The I²C bus supports Standard-Mode, Fast-Mode and High Speed Mode.
5. User selectable via ODR control register setting
6. Start up time is from PC1 set to valid outputs. Time varies with Output Data Rate (ODR) and mode setting (RES); see diagrams below

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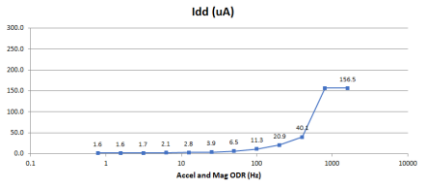
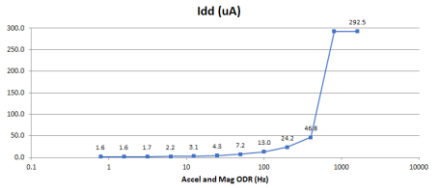
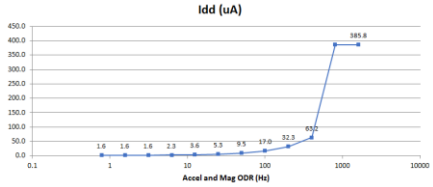
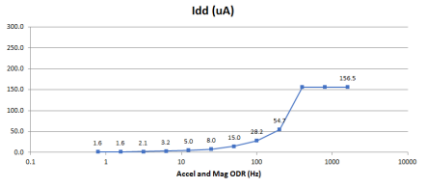
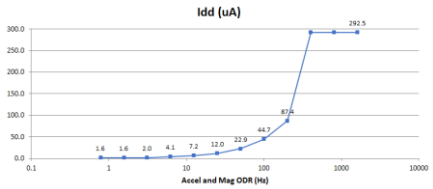
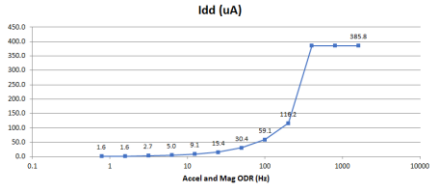
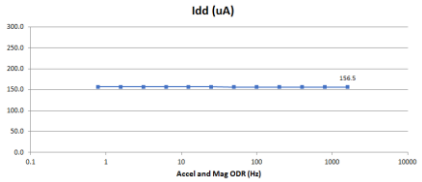
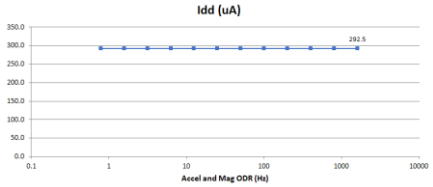
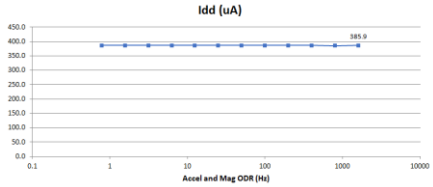
Current Consumption Diagrams

Typical current over selected ODR (0.781,1.563,3.125,6.25,12.5,25,50,100,200,400,800,1600Hz) @ VDD = 2.5V and T = 25ºC

Res	Accel Only	Mag Only	Accel and Mag
00			
01			
10, 11			

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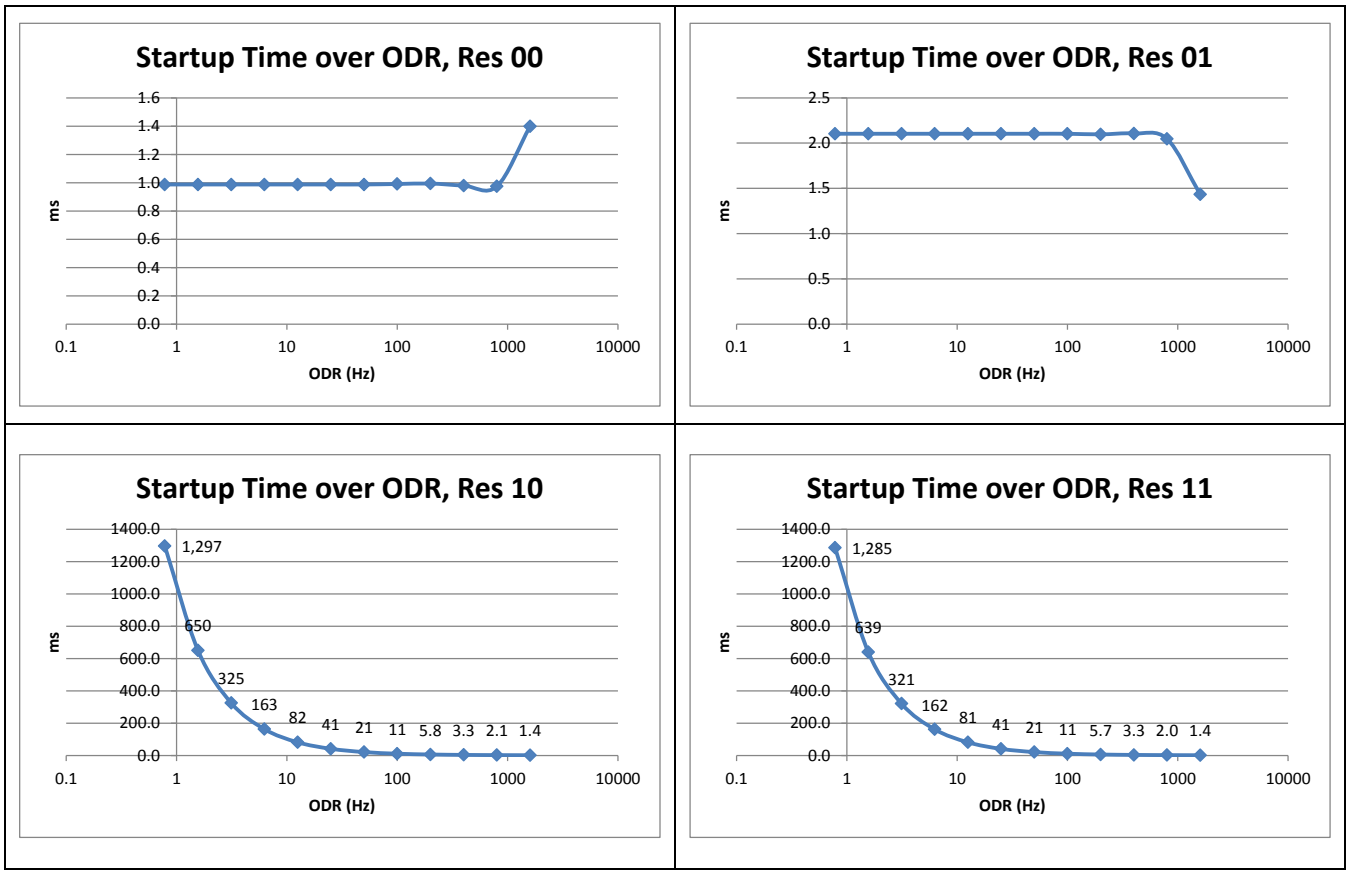
Start Up Time Diagrams

Typical Start Up Time over selected ODR (0.781,1.563,3.125,6.25,12.5,25,50,100,200,400,800,1600Hz)



Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD, VDD_{Low}**, **T_{VDD}** (rise time), and **T_{Vdd_Off}** profile of individual applications. It is recommended to minimize **VDD_{Low}**, and **T_{VDD}**, and maximize **T_{Vdd_Off}**. It is also advised that the VDD ramp up time **T_{Vdd}** be monotonic. To assure proper POR in all environmental conditions the application should be evaluated over the range of **VDD, VDD_{Low}**, **T_{VDD}** **,** **T_{Vdd_Off}** and temperature as POR performance can vary depending on these parameters. In order to guarantee proper reset regardless of the **VDD_{Low}**, **T_{VDD}** (rise time), and **T_{Vdd_Off}** parameters, a software reset can be issued via the I2C protocol. Please refer to Technical Note ***TN005 KMX62 Power-On Procedure*** to ensure proper POR function in your application.

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I²C Timing Diagram

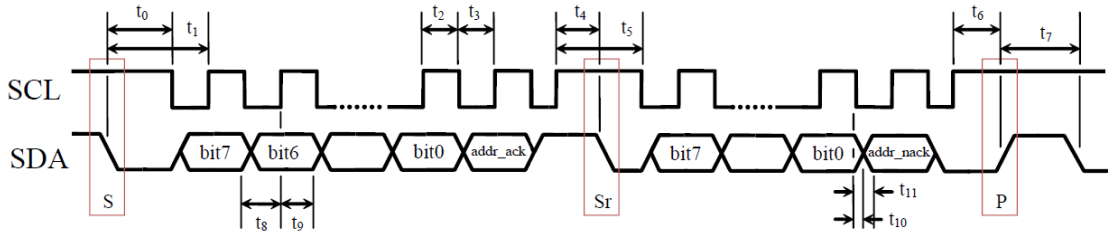

Table 4. I²C Timing (Fast Mode)

Number	Description	MIN	MAX	Units
t_0	SDA low to SCL low transition (Start event)	50	-	ns
t_1	SDA low to first SCL rising edge	100	-	ns
t_2	SCL pulse width: high	100	-	ns
t_3	SCL pulse width: low	100	-	ns
t_4	SCL high before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: high during a S/Sr/P event	100	-	ns
t_6	SCL high before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: high	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I²C CLK	2.5	-	us

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Environmental Specifications

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Absolute Limits	V	-0.3	-	3.6
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Table 5. Environmental Specifications

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

The products described above conform to RoHS Directive 2011/65/EU of the European Parliament and of the Council of the European Union that was issued June 8, 2011. Specifically, these products do not contain any non-exempted amounts of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are “of uniform composition throughout”. The MCV for lead, mercury, hexavalent chromium, PBB, and PBDE is 0.10%. The MCV for cadmium is 0.010%.

Applicable Exemption: *7C-I - Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors (piezoelectronic devices) or in a glass or ceramic matrix compound.*

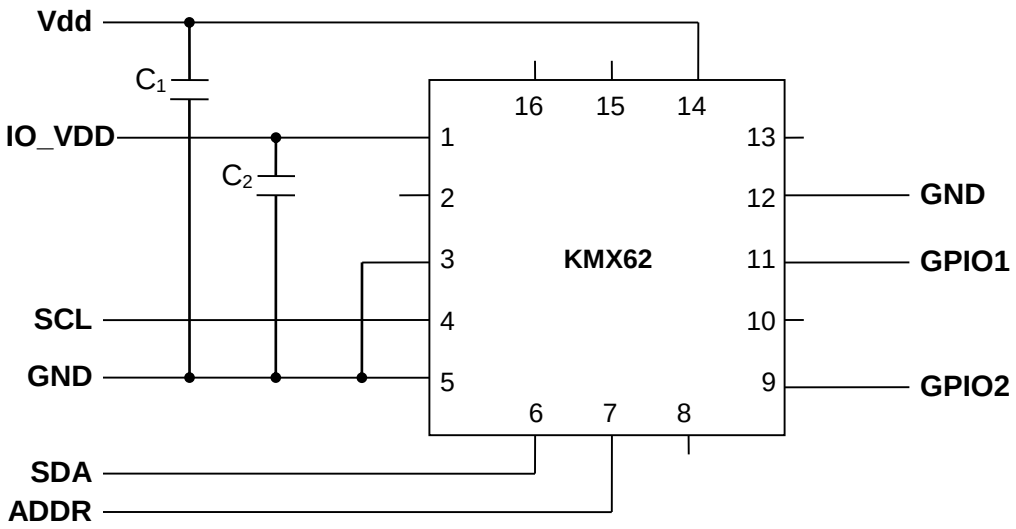
These products are also in conformance with REACH Regulation No 1907/2006 of the European Parliament and of the Council that was issued Dec. 30, 2011. They do not contain any Substances of Very High Concern (SVHC-161) as identified by the European Chemicals Agency as of 17 December 2014.

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

Application Schematic



Pin Descriptions

Pin	Name	Description
1	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
2	CAP	Do not connect. Must be left floating.
3	GND	Ground
4	SCL	I^2C Serial Clock
5	GND	Ground
6	SDA	I^2C Serial Data
7	ADDR	I^2C Address pin.This pin must be connected to IO_VDD or GND to determine the I2C Device Address.
8	NC	Not Internally Connected
9	GPIO2	GPIO 2. Cannot float when configured as an input.
10	NC	Not Internally Connected
11	GPIO1	GPIO 1. Cannot float when configured as an input.
12	GND	Ground
13	NC	Not Internally Connected
14	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
15	NC	Not Internally Connected
16	NC	Not Internally Connected

Table 6. KMX62 Pin Descriptions

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Package Dimensions and Orientation

Dimensions

3 x 3 x 0.9 mm LGA

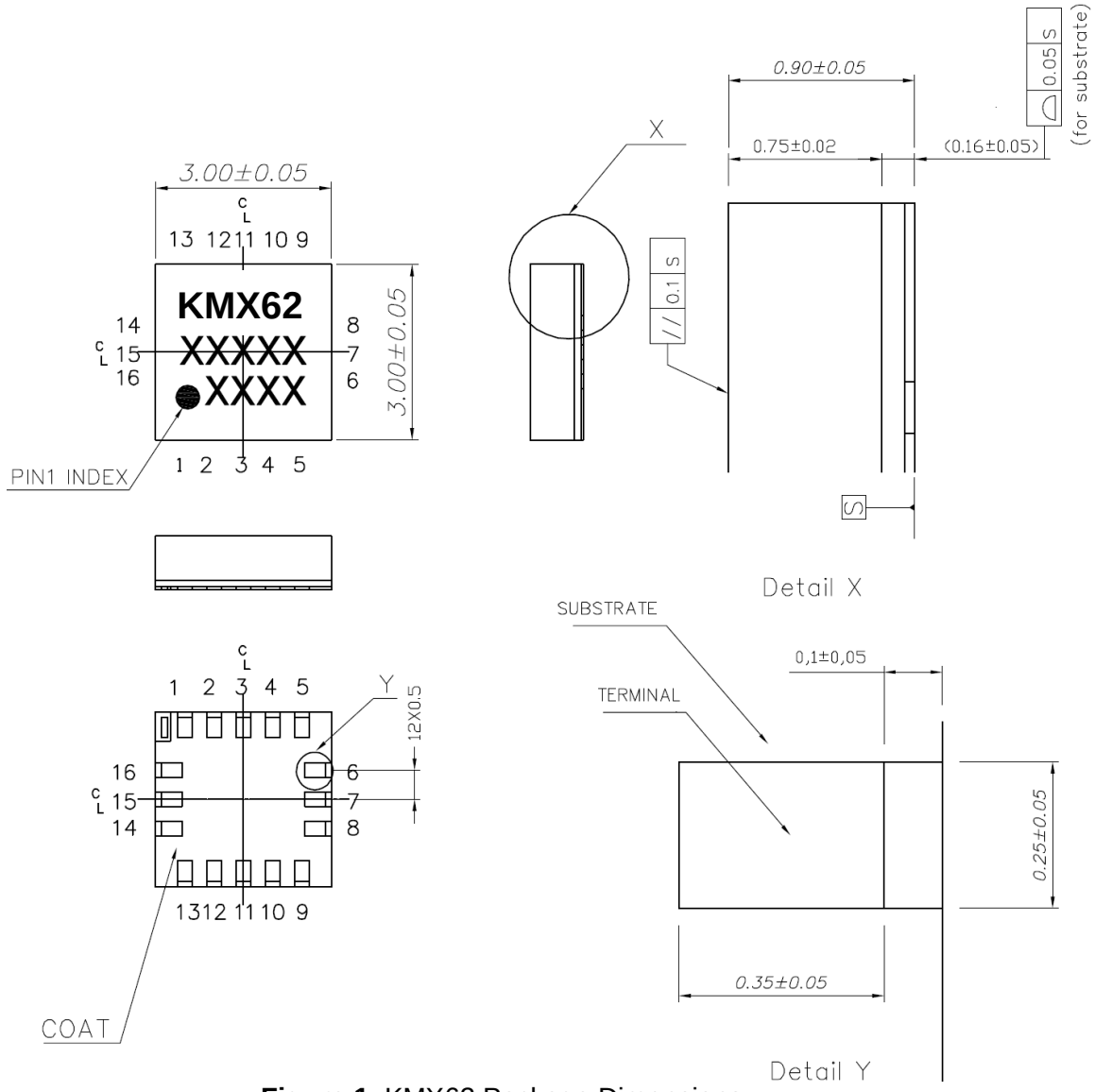

Figure 1. KMX62 Package Dimensions

Orientation

When device is moved in +X, +Y, or +Z direction, the corresponding accelerometer output will increase. When the +X, +Y, or +Z arrow is directed toward North, the output of that axis is positive.

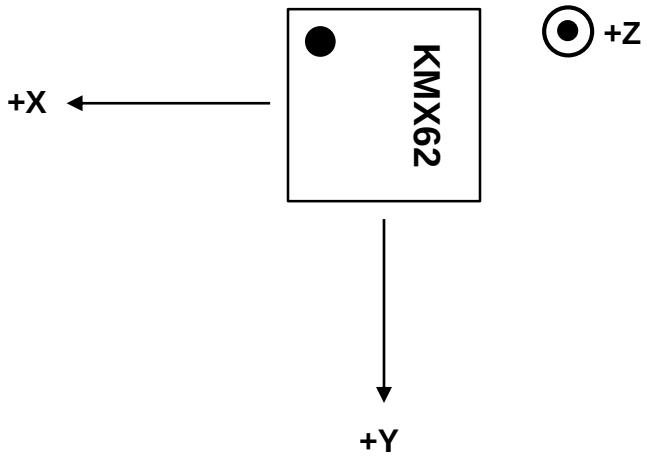

Figure 2. KMX62 Orientation

Please avoid mounting this product on the part in which magnetic field disturbance exists, such as near any parts containing ferrous materials.

Digital Interface

The Kionix KMX62 digital sensor has the ability to communicate on the I²C digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system processors. The I2C interface is compliant with high-speed mode, fast mode and standard mode I2C protocols.

The serial interface terms and descriptions as indicated in Table 7 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 7. Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KMX62 has the ability to communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The system Master provides the serial clock signal and addresses Slave devices on the bus. The KMX62 always operates as a Slave device during standard Master-Slave I²C operation.

I²C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I²C bus is considered free when both lines are high.

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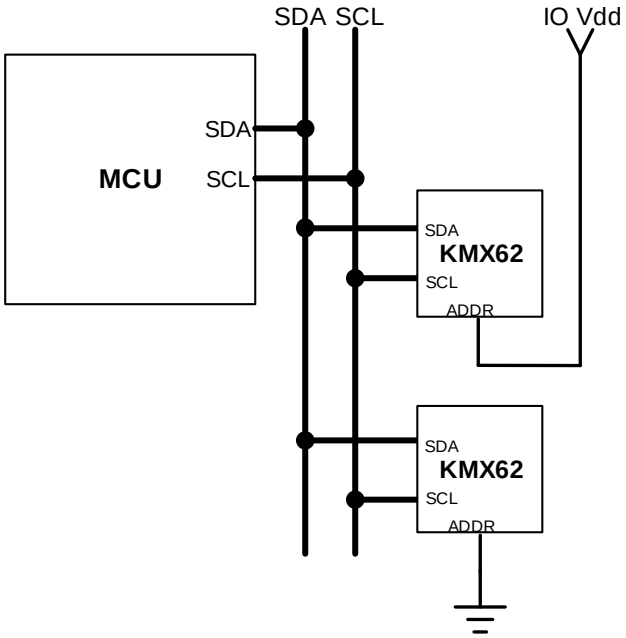

Figure 3. Multiple KMX62 I²C Connection

Description	Address Pad	7 bit Address	Address	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
I2C Wr	IO_VDD	0Fh	1Eh	0	0	0	1	1	1	1	0
I2C Rd	IO_VDD	0Fh	1Fh	0	0	0	1	1	1	1	1
I2C Wr	GND	0Eh	1Ch	0	0	0	1	1	1	0	0
I2C Rd	GND	0Eh	1Dh	0	0	0	1	1	1	0	1

Table 8. I²C Address

I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally-stored address. If they match, the device considers itself addressed by the Master. The KMX62's Slave Address is comprised of two programmable

parts, which allows for connection of multiple KMX62's to the same I^2C bus. The LSB is determined by the assignment of ADDR to GND or IO_Vdd. Figure 3 and Table 8 above show how two KMX62's would be implemented on an I^2C bus.

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I^2C bus is now free. Note that if the KMX62 is accessed through I^2C protocol before the startup is finished a NACK signal is sent.

Writing to a KMX62 8-bit Register

Upon power up, the Master must write to the KMX62's control registers to set its operational mode. Therefore, when writing to a control register on the I^2C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KMX62 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KMX62 to which 8-bit register the Master will be writing the data. Since this is I^2C mode, the MSB of the RA command should always be zero (0). The KMX62 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KMX62 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KMX62 is now stored in the appropriate register. The KMX62 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

Reading from a KMX62 8-bit Register

When reading data from a KMX62 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KMX62 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KMX62 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KMX62 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. The KMX62 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page. Reading data from a buffer read register is a special case because if register address (RA) is set to buffer read register (BUF_READ) in Sequence 4, the register auto-increment feature is automatically disabled. Instead, the Read Pointer will increment to the next data in the buffer, thus allowing reading multiple bytes of data from the buffer using a single SAD+R command.

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Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I^2C bus and how the Master and Slave interact during these transfers. Table 9 defines the I^2C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 9. I^2C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

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HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5. HS-mode data transfer of the Master writing one byte to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	S	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

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Power Modes

The KMX62 has five power modes: Off, Stand-by, Sleep, Low Power (RES = 0) and High Resolution (RES = 1). The part exists in one of these five modes at any given time. Off and Stand-by modes have very low current consumptions.

Power Mode	Bus State	IO_VDD	VDD	Function	Outputs
Off	-	OFF	OFF	No sensor activity	Not available
		ON	OFF		
		OFF	ON		
Stand-by	Active	ON	ON	Waiting activation command	Not available
Sleep	Active	ON	ON	Accelerometer active looking for motion wake up	Accel registers only – no buffer, no DRDY int
<RES> = 00 or 01	Active	ON	ON	All functionalities available	All sensors available
<RES> = 10 or 11	Active	ON	ON	All functionalities available	All sensors available

Off mode

One or both of the power supplies (VDD or IO_VDD) are not powered. The sensor is completely inactive and not reporting or communicating. Bus communication actions of other devices are not disturbed if they are using the same bus interface as this component.

Initial Startup

The preferred startup sequence is to turn on IO_VDD before VDD, but if VDD is turned on first, the component will not affect the bus communications (no latch-up or other problems during engine system level wake-up).

Power On Reset (POR) is performed every time when:

1. IO_VDD supply is valid
2. VDD power supply is going to valid level

OR

1. IO_VDD power supply is going to valid level
2. VDD supply is valid

When POR occurs, the registers are loaded from OTP and the part is put into Stand-by mode.

Stand-by mode

The primary function of the stand-by mode is to ensure fast wake-up to active mode and to minimize current consumption. This mode is set as default when both power supplies are applied and the POR function occurs. A Soft Reset command also performs the POR function and puts the part into Stand-by mode.

Stand-by mode is a low power waiting state for fast turn on time. Bus communication actions of other components are not disturbed if they are using the same bus. There is only one possible way to change to active mode – a register command from the external application processor via the I^2C bus.

Sleep mode

While in sleep mode, the accelerometer is periodically taking a measurement to detect if there is any motion. Data in the accelerometer registers is being updated, however, there is no data ready interrupt being reported. Also, no data is being sent to the buffer.

Low Power (<RES> = 00 or 01) mode

Stand-by-mode can be changed to a Low Power mode by writing to register Control Register 2 or when a motion wake up event occurs.

Low power mode engages the full functionality of accelerometer and/or magnetometer measurements in a low power, low resolution mode. The host has the ability to change settings in the control register back to Stand-by mode for either or both the accelerometer and magnetometer. If enabled, the back to sleep function will put the part into the Sleep mode.

The host can also place the part into High Resolution (<RES> = 10 or 11) mode by writing to Control Register 2.

High Resolution (<RES> = 10 or 11) mode

Stand-by-mode can be changed to High Resolution mode by writing to register Control Register 2.

High Resolution mode engages the full functionality of accelerometer and/or magnetometer measurements in a higher power, higher resolution mode. The host has the ability to change settings in the control register back to Stand-by mode for either or both the accelerometer and magnetometer. If enabled, the back to sleep function will put the part into the Sleep mode.

The host can also place the part into Low Power (<RES> = 00 or 01) mode by writing to Control Register 2.

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Embedded Registers

The KMX62 has 45 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and also describes bit functions of each register. Table 10 below provides a listing of the accessible 8-bit registers and their addresses.

Register Name	I^2C Address (Hex)	Type R/W
WHO_AM_I	00h	R/W
INS1	01h	R
INS2	02h	R
INS3	03h	R
INL	05h	R
ACCEL_XOUT_L	0Ah	R
ACCEL_XOUT_H	0Bh	R
ACCEL_YOUT_L	0Ch	R
ACCEL_YOUT_H	0Dh	R
ACCEL_ZOUT_L	0Eh	R
ACCEL_ZOUT_H	0Fh	R
MAG_XOUT_L	10h	R
MAG_XOUT_H	11h	R
MAG_YOUT_L	12h	R
MAG_YOUT_H	13h	R
MAG_ZOUT_L	14h	R
MAG_ZOUT_H	15h	R
TEMP_OUT_L	16h	R
TEMP_OUT_H	17h	R
INC1	2Ah	R/W
INC2	2Bh	R/W
INC3	2Ch	R/W
INC4	2Dh	R/W
INC5	2Eh	R/W

Register Name	I^2C Address (Hex)	Type R/W
AMI_CNTL1	2Fh	R/W
AMI_CNTL2	30h	R/W
AMI_CNTL3	31h	R/W
MMI_CNTL1	32h	R/W
MMI_CNTL2	33h	R/W
MMI_CNTL3	34h	R/W
FFI_CNTL1	35h	R/W
FFI_CNTL2	36h	R/W
FFI_CNTL3	37h	R/W
ODCNTL	38h	R/W
CNTL1	39h	R/W
CNTL2	3Ah	R/W
COTR	3Ch	R
BUF_CTRL_1	77h	R/W
BUF_CTRL_2	78h	R/W
BUF_CTRL_3	79h	R/W
BUF_CLEAR	7Ah	W
BUF_STATUS_1	7Bh	R
BUF_STATUS_2	7Ch	R
BUF_STATUS_3	7Dh	R
BUF_READ	7Eh	R

Table 10. I2C Register Map

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Register Descriptions

Register	Addr	R/W	POR	Wrt	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0

Register *is the general description of the contents of the register.*

Addr *is the address of the register used during communications*

R/W *describes if a register can be written to or read from.*

POR *gives the value of the register after power is applied or after software reset (SRST bit)*
OTP = Factory default values reloaded into registers from OTP.
00h = Register contains all zeros
blank = Register is a write only register or sensor output

Wrt *describes how the ASIC will behave if the register is written while enabled. This is important because if modes of operation are change while the state machine is running the digital portion of the ASIC can enter undefined states and cause unexpected results.*
blank = This register cannot be written to.
OTF = On The Fly registers can be written while the ASIC is enabled and the change will be accepted with no interruption in the operation although there will be a settling time for some changes.
RST = Restart indicates that if this register is written to while any sensors are enabled the ASIC will automatically disable for a brief time and then re-enable the sensors that were previously enabled. Interrupt and buffer status registers will be cleared (01h, 02h, 03h, 7Bh, 7Ch, 7Dh)
NRST = No Restart indicates that if this register is written to while any sensors are enabled the ASIC will NOT automatically disable/enable. Changes apply to the block being controlled for quick sweeps but the operation of the digital engine may not be correct and the DUT must be disabled/enabled for complete functionality.

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WHO_AM_I

This register can be used for supplier recognition, as it can be factory written to a known byte value.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
WHO_AM_I	00h	R/W	18h	OTF	WAI_MIR<7>	WAI_MIR<6>	WAI_MIR<5>	WAI_MIR<4>	WAI_MIR<3>	WAI_MIR<2>	WAI_MIR<1>	WAI_MIR<0>

INS1 - Interrupt Source Register 1

This register tells which function caused an interrupt.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
INS1	01h	R	00h		INT	BFI	WMI	DRDY_A	DRDY_M	FFI	AMI	MMI

INT *reports the combined (OR) interrupt information of all enabled interrupt.*
0= no interrupt event, 1= interrupt event has occurred.

BFI *- indicates that the buffer is full. This bit is cleared when the data is read until the buffer is not full.*
BFI = 0 – Buffer is not full
BFI = 1 – Buffer is full

WMI *- indicates that user-defined buffer watermark has been reached. This bit is cleared when the data is read until the sample level in the buffer is smaller than the watermark threshold.*
WMI = 0 – Buffer watermark not reached
WMI = 1 – Buffer watermark reached

DRDY_A *- indicates that new acceleration data is available. This bit is cleared when the data is read or the interrupt release register (INL Register) is read.*
DRDY = 0 – New acceleration data not available
DRDY = 1 – New acceleration data available

DRDY_M *- indicates that new magnetometer data is available. This bit is cleared when the data is read or the interrupt release register (INL Register) is read.*
DRDY = 0 – New acceleration data not available
DRDY = 1 – New acceleration data available

FFI *– Free fall, this bit is cleared when the interrupt source latch register (INL Register) is read.*
FFS = 1 – Free fall has activated the interrupt
FFS = 0 – No free fall

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AMI *– Accelerometer motion interrupt, This bit is cleared when the interrupt source latch register (INL Register) is read.*
AMS = 1 – Motion has activated the interrupt
AMS = 0 – No motion
MMI *– Magnetometer motion interrupt, This bit is cleared when the interrupt source latch register (INL Register) is read.*
MMS = 1 – Motion has activated the interrupt
MMS = 0 – No motion

INS2 - Interrupt Source Register 2

This register reports the sensor, axis and direction of the motion that triggered the interrupt.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
INS2	02h	R	00h		SPARE_0002<7>	SPARE_0002<6>	AXNI	AXPI	AYNI	AYPI	AZNI	AZPI

AXNI *- x negative (x-)*
AXPI *- x positive (x+)*
AYNI *- y negative (y-)*
AYPI *- y positive (y+)*
AZNI *- z negative (z-)*
AZPI *- z positive (z+)*

INS3 - Interrupt Source Register 3

The Interrupt Source Register 3 reports the sensor, axis and direction of the motion that triggered the interrupt.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
INS3	03h	R	00h		SPARE_0003<7>	SPARE_0003<6>	MXNI	MXPI	MYNI	MYPI	MZNI	MZPI

MXNI *- x negative (x-)*
MXPI *- x positive (x+)*
MYNI *- y negative (y-)*
MYPI *- y positive (y+)*
MZNI *- z negative (z-)*
MZPI *- z positive (z+)*

INL - Interrupt Latch Release

Latched interrupt source information (at INS1 and INS2) is cleared and physical interrupt latched pin is changed to its inactive state when this register is read. If an engine is configured as an unlatched interrupt and the current state is indicating and interrupt this release will not clear the interrupt.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
INL	05h	R	00h		0	0	0	0	0	0	0	0

Accelerometer output

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
ACCEL_XOUT_L	0Ah	R			ACC_X<7>	ACC_X<6>	ACC_X<5>	ACC_X<4>	ACC_X<3>	ACC_X<2>	ACC_X<1>	ACC_X<0>
ACCEL_XOUT_H	0Bh	R			ACC_X<15>	ACC_X<14>	ACC_X<13>	ACC_X<12>	ACC_X<11>	ACC_X<10>	ACC_X<9>	ACC_X<8>
ACCEL_YOUT_L	0Ch	R			ACC_Y<7>	ACC_Y<6>	ACC_Y<5>	ACC_Y<4>	ACC_Y<3>	ACC_Y<2>	ACC_Y<1>	ACC_Y<0>
ACCEL_YOUT_H	0Dh	R			ACC_Y<15>	ACC_Y<14>	ACC_Y<13>	ACC_Y<12>	ACC_Y<11>	ACC_Y<10>	ACC_Y<9>	ACC_Y<8>
ACCEL_ZOUT_L	0Eh	R			ACC_Z<7>	ACC_Z<6>	ACC_Z<5>	ACC_Z<4>	ACC_Z<3>	ACC_Z<2>	ACC_Z<1>	ACC_Z<0>
ACCEL_ZOUT_H	0Fh	R			ACC_Z<15>	ACC_Z<14>	ACC_Z<13>	ACC_Z<12>	ACC_Z<11>	ACC_Z<10>	ACC_Z<9>	ACC_Z<8>

These registers contain up to 16-bits of valid acceleration data for each axis. The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per **Figure 4** below. The register acceleration output binary data is represented in N-bit 2's complement format. For example, if N = 16 bits, then the Counts range is from -32768 to 32767.

16-bit Register Data (2's complement)	**Equivalent Counts in decimal**	**Range = +/-2g**	**Range = +/-4g**	**Range = +/-8g**	**Range = +/-16g**
0111 1111 1111 1111	32767	+1.99994g	+3.99988g	+7.99976g	+15.99951g
0111 1111 1111 1110	32766	+1.99988g	+3.99976g	+7.99951g	+15.99902g
…	…	…	…	…	…
0000 0000 0000 0001	1	+0.00006g	+0.00012g	+0.00024g	+0.00049g
0000 0000 0000 0000	0	0.00000g	0.00000g	0.000g	0.00000g
1111 1111 1111 1111	-1	-0.00006g	-0.00012g	-0.00024g	-0.00049g
…	…	…	…	…	…
1000 0000 0000 0001	-32767	-1.99994g	-3.99988g	-7.99976g	-15.99951g
1000 0000 0000 0000	-32768	-2.00000g	-4.00000g	-8.00000g	-16.00000g

Figure 4. Acceleration (g) Calculation

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Magnetometer output

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
MAG_XOUT_L	10h	R			MAG_X<7>	MAG_X<6>	MAG_X<5>	MAG_X<4>	MAG_X<3>	MAG_X<2>	MAG_X<1>	MAG_X<0>
MAG_XOUT_H	11h	R			MAG_X<15>	MAG_X<14>	MAG_X<13>	MAG_X<12>	MAG_X<11>	MAG_X<10>	MAG_X<9>	MAG_X<8>
MAG_YOUT_L	12h	R			MAG_Y<7>	MAG_Y<6>	MAG_Y<5>	MAG_Y<4>	MAG_Y<3>	MAG_Y<2>	MAG_Y<1>	MAG_Y<0>
MAG_YOUT_H	13h	R			MAG_Y<15>	MAG_Y<14>	MAG_Y<13>	MAG_Y<12>	MAG_Y<11>	MAG_Y<10>	MAG_Y<9>	MAG_Y<8>
MAG_ZOUT_L	14h	R			MAG_Z<7>	MAG_Z<6>	MAG_Z<5>	MAG_Z<4>	MAG_Z<3>	MAG_Z<2>	MAG_Z<1>	MAG_Z<0>
MAG_ZOUT_H	15h	R			MAG_Z<15>	MAG_Z<14>	MAG_Z<13>	MAG_Z<12>	MAG_Z<11>	MAG_Z<10>	MAG_Z<9>	MAG_Z<8>

These registers contain 16-bits of valid magnetic field data for each axis. The data is protected from overwrite during each read, and can be converted from digital counts to magnetic field strength (μT) per Figure 5 below.

16-bit Data	Magnetic field μT
0111 1111 1111 1111	+1199.9634 μT
0111 1111 1111 1110	+1199.9268 μT
…	…
…	…
0000 0000 0000 0001	+0.0366 μT
0000 0000 0000 0000	0 μT
1111 1111 1111 1111	-0.0366 μT
…	…
…	…
1000 0000 0000 0001	-1199.9634 μT
1000 0000 0000 0000	-1200.0000 μT

Figure 5. Magnetic field (μT) Calculation

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Temperature Output

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
TEMP_OUT_L	16h	R			TEMP<7>	TEMP<6>	TEMP<5>	TEMP<4>	TEMP<3>	TEMP<2>	TEMP<1>	TEMP<0>
TEMP_OUT_H	17h	R			TEMP<15>	TEMP<14>	TEMP<13>	TEMP<12>	TEMP<11>	TEMP<10>	TEMP<9>	TEMP<8>

The temperature registers contain up to 16-bits of temperature data. If only register TEMP_OUT_H is used, then the sensitivity can be considered as 1 count/°C. If both registers TEMP_OUT_H and TEMP_OUT_L are used (16 bits), then sensitivity can be considered as 256 count/°C.

8-bit Register Data TEMP_OUT_H (2's complement)	**Equivalent Counts in decimal**	**Temperature (°C)**
0101 0101	85	+85 °C
…	…	…
0000 0001	1	+1 °C
0000 0000	0	0 °C
1111 1111	-1	-1 °C
…	…	…
1101 1000	-40	-40 °C

16-bit Register Data (2's complement)	**Equivalent Counts in decimal**	**Temperature (°C)**
0101 0101 0000 0000	21760	+85.000 °C
…	…	…
0000 0001 0000 0000	256	+1.0000 °C
…	…	…
0000 0000 0100 0000	64	+0.2500 °C
…	…	…
0000 0000 0000 0001	1	+0.0039 °C
0000 0000 0000 0000	0	0.0000 °C
1111 1111 1111 1111	-1	-0.0039 °C
…	…	…
1111 1111 1100 0000	-64	-0.2500 °C
…	…	…
1111 1111 0000 0000	-256	-1.0000 °C
…	…	…
1101 1000 0000 0000	-10240	-40.000 °C

Figure 6. Temperature (°C) Calculation

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INC1 - Interrupt Control 1

This register controls routing of an interrupt reporting to physical interrupt pin GPIO1.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
INC1	2Ah	R/W	00h	RST	SPARE_002A<7>	BFI1	WMI1	DRDY_A1	DRDY_M1	FFI1	AMI1	MMI1

BFI1 - *Buffer full interrupt reported on GPIO1*
BFI = 0 – disable
BFI = 1 – enable.
WMI1 *- Watermark interrupt reported on GPIO1*
WMI1 = 0 – disable
WMI1 = 1 – enable
DRDY_A1 *- Accelerometer Data ready reported on GPIO1*
DRDY_A1 = 0 – disable
DRDY_A1 = 1 – enable.
DRDY_M1 *- Magnetometer Data ready reported on GPIO1*
DRDY_M1 = 0 – disable
DRDY_M1 = 1 – enable.
FFI1 *- Accelerometer Freefall interrupt reported on GPIO1*
FFI1 = 0 – disable
FFI1 = 1 – enable.
AMI1 *- Accelerometer motion interrupt reported on GPIO1*
AMI1 = 0 – disable
AMI1 = 1 – enable.
MMI1 *- Magnetometer motion interrupt reported on GPIO1*
MMI1 = 0 – disable
MMI1 = 1 – enable.

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INC2 - Interrupt Control 2

This register controls routing of an interrupt reporting to physical interrupt pin GPIO2.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
INC2	2Bh	R/W	00h	RST	SPARE_002B<7>	BFI2	WMI2	DRDY_A2	DRDY_M2	FFI2	AMI2	MMI2

BFI2- *Buffer full interrupt reported on GPIO2*
BFI2 = 0 – disable
BFI2 = 1 – enable.
WMI2 *- Watermark interrupt reported on GPIO2*
WMI2 = 0 – disable
WMI2 = 1 – enable
DRDY_A2 *- Accelerometer Data ready reported on GPIO2*
DRDY_A2 = 0 – disable
DRDY_A2 = 1 – enable.
DRDY_M2 *- Magnetometer Data ready reported on GPIO2*
DRDY_M2 = 0 – disable
DRDY_M2 = 1 – enable.
FFI2 *- Accelerometer Freefall interrupt reported on GPIO2*
FFI2 = 0 – disable
FFI2 = 1 – enable.
AMI2 *- Accelerometer motion interrupt reported on GPIO2*
AMI2 = 0 – disable
AMI2 = 1 – enable.
MMI2 *- Magnetometer motion interrupt reported on GPIO2*
MMI2 = 0 – disable
MMI2 = 1 – enable.

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INC3 – Interrupt Control 3

This register controls the GPIO pin configuration.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
INC3	2Ch	R/W	88h	RST	IED2	IEA2	IEL2<1>	IEL2<0>	IED1	IEA1	IEL1<1>	IEL1<0>

IED1 *– Interrupt pin drive options for GPIO1*
IED1 = 0 – push-pull
IED1 = 1 – open-drain
IEA1 *- Interrupt active level control for interrupt GPIO1*
IEA1 = 0 – active low
IEA1 = 1 – active high
IEL1 <1,0>*- Interrupt latch control for interrupt GPIO1*
IEL1 = 0,0 – latched/unlatched. Unlatched feature is available for FFI,MME and AMI.
IEL1 = 0,1 – pulsed. In pulse mode the pulse width is 50us for normal mode and 10us for debug mode (high ODR rates).
IEL1 = 1,X – trigger input for FIFO.
IED2 *– Interrupt pin drive options for GPIO2*
IED2 = 0 – push-pull
IED2 = 1 – open-drain
IEA2 *- Interrupt active level control for interrupt GPIO2*
IEA2 = 0 – active low
IEA2 = 1 – active high
IEL2 <1,0>*- Interrupt latch control for interrupt GPIO2*
IEL2 = 0,0 – latched/unlatched. Unlatched feature is available for FFI,MME and AMI.
IEL2 = 0,1 – pulsed. In pulse mode the pulse width is 50us for normal mode and 10us for debug mode (high ODR rates).
IEL2 = 1,X – trigger input for FIFO.

IED#	IEA#	IEL#<1,0>	BFI#	WMI#	DRDY_A#	DRDY_M#	FFI#	MMI#	AMI#	GPIO state
0	0	0,0	0	0	0	0	0	0	0	The GPIO pin is held high
0	0	0,1	0	0	0	0	0	0	0	The GPIO pin is held high
0	1	0,0	0	0	0	0	0	0	0	The GPIO pin is held low
0	1	0,1	0	0	0	0	0	0	0	The GPIO pin is held low
1	0	0,0	0	0	0	0	0	0	0	The GPIO pin is high impedance
1	0	0,1	0	0	0	0	0	0	0	The GPIO pin is high impedance
1	1	0,0	0	0	0	0	0	0	0	The GPIO pin is held low
1	1	0,1	0	0	0	0	0	0	0	The GPIO pin is held low
X	X	1,X	X	X	X	X	X	X	X	The GPIO pin is configured as an input for FIFO trigger. If both GPIO pins are trigger, the signals are OR'ed.

Special Cases

INC4 - Interrupt Control 4

This register controls which accelerometer axis and direction of detected motion can cause an interrupt.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
INC4	2Dh	R/W	3Fh	N	SPARE_002D<7>	SPARE_002D<6>	AXNIE	AXPIE	AYNIE	AYPIE	AZNIE	AZPIE

AXNIE *- x negative (x-) accelerometer mask for AMI, 0=disable, 1=enable.*
AXPIE *- x positive (x+) accelerometer mask for AMI, 0=disable, 1=enable.*
AYNIE *- y negative (y-) accelerometer mask for AMI, 0=disable, 1=enable.*
AYPIE *- y positive (y+) accelerometer mask for AMI, 0=disable, 1=enable.*
AZNIE *- z negative (z-) accelerometer mask for AMI, 0=disable, 1=enable.*
AZPIE *- z positive (z+) accelerometer mask for AMI, 0=disable, 1=enable.*

INC5 - Interrupt Control 5

This register controls which magnetometer axis and direction of detected motion can cause an interrupt.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
INC5	2Eh	R/W	3Fh	N	SPARE_002E<7>	SPARE_002E<6>	MXNIE	MXPIE	MYNIE	MYPIE	MZNIE	MZPIE

MXNIE *- x negative (x-) magnetometer mask for MMI, 0=disable, 1=enable.*
MXPIE *- x positive (x+) magnetometer mask for MMI, 0=disable, 1=enable.*
MYNIE *- y negative (y-) magnetometer mask for MMI, 0=disable, 1=enable.*
MYPIE *- y positive (y+) magnetometer mask for MMI, 0=disable, 1=enable.*
MZNIE *- z negative (z-) magnetometer mask for MMI, 0=disable, 1=enable.*
MZPIE *- z positive (z+) magnetometer mask for MMI, 0=disable, 1=enable.*

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AMI_CNTL1 - Accelerometer Motion Control 1

This register has control settings for the accelerometer motion interrupt function.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
AMI_CNTL1	2Fh	R/W	00h	RST	AMITH<7>	AMITH<6>	AMITH<5>	AMITH<4>	AMITH<3>	AMITH<2>	AMITH<1>	AMITH<0>

AMITH<7:0> *- Accelerometer motion interrupt threshold. This value is compared to the top 8 bits of the accelerometer 4g output.*

AMI_CNTL2 - Accelerometer Motion Control 2

This register has control settings for the accelerometer motion interrupt function.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
AMI_CNTL2	30h	R/W	00h	RST	AMICT<7>	AMICT<6>	AMICT<5>	AMICT<4>	AMICT<3>	AMICT<2>	AMICT<1>	AMICT<0>

AMICT<7:0> *- Accelerometer motion interrupt counter. Every count is calculated as 1/ODR delay period, where the Motion Interrupt ODR is user-defined per the OAMI bits in AM_CNTL3. A new state must be valid as many measurement periods before the change is accepted. Note that to properly change the value of this register, the accelerometer should be in stand.*

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AMI_CNTL3 - Accelerometer Motion Control 3

This register has control settings for the accelerometer motion interrupt function.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
AMI_CNTL3	31h	R/W	00h	RST	AMI_EN	AMIUL	SPARE_0031<5>	SPARE_0031<4>	SPARE_0031<3>	OAMI<2>	OAMI<1>	OAMI<0>

AMI_EN *- Accelerometer motion interrupt engine enable*

AMI_EN = 0 – disabled

AMI_EN = 1 – enabled

AMIUL *- Accelerometer Motion Interrupt latch/un-latch control for interrupt GPIO1/2*

AMIUL = 0 – latched

AMIUL = 1 – un-latched

OAMI<2:0> *- Output Data Rate at which the accelerometer motion detection performs its function.*

OAMI<2>	OAMI <1>	OAMI <0>	Output Data Rate (Hz)
0	0	0	0.781
0	0	1	1.563
0	1	0	3.125
0	1	1	6.25
1	0	0	12.5
1	0	1	25
1	1	0	50
1	1	1	100

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MMI_CNTL1 - Magnetometer Motion Control 1

This register has control settings for the magnetometer motion interrupt function.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
MMI_CNTL1	32h	R/W	00h	RST	MMITH<7>	MMITH<6>	MMITH<5>	MMITH<4>	MMITH<3>	MMITH<2>	MMITH<1>	MMITH<0>

MMITH<7:0> *- Magnetometer motion interrupt threshold. This value is compared to the top 8 bits of the magnetometer 1200uT output.*

MMI_CNTL2 - Magnetometer Motion Control 2

This register has control settings for the magnetometer motion interrupt function.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
MMI_CNTL2	33h	R/W	00h	RST	MMICT<7>	MMICT<6>	MMICT<5>	MMICT<4>	MMICT<3>	MMICT<2>	MMICT<1>	MMICT<0>

MMICT<7:0> *- Magnetometer motion interrupt counter. Every count is calculated as 1/ODR delay period.*

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MMI_CNTL3 - Magnetometer Motion Control 3

This register has control settings for the magnetometer motion interrupt function.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
MMI_CNTL3	34h	R/W	00h	RST	MMI_EN	MMIUL	SPARE_0034<5>	SPARE_0034<4>	SPARE_0034<3>	OMMI<2>	OMMI<1>	OMMI<0>

MMI_EN - *Magnetometer motion interrupt engine enable*
MMI_EN = 0 – disabled
MMI_EN = 1 – enabled

MMIUL - *Magnetometer Motion Interrupt latch/un-latch control for interrupt GPIO1/2*
MMIUL = 0 – latched
MMIUL = 1 – un-latched

OMMI<2:0> - *Output Data Rate at which the magnetometer motion detection performs its function.*

OMMI<2>	OMMI <1>	OMMI <0>	Output Data Rate (Hz)
0	0	0	0.781
0	0	1	1.563
0	1	0	3.125
0	1	1	6.25
1	0	0	12.5
1	0	1	25
1	1	0	50
1	1	1	100

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FFI_CNTL1 - Free Fall Control 1

This register has control settings for the free fall interrupt function.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
FFI_CNTL1	35h	R/W	00h	RST	FFITH<7>	FFITH<6>	FFITH<5>	FFITH<4>	FFITH<3>	FFITH<2>	FFITH<1>	FFITH<0>

FFITH<7:0> *- Accelerometer free fall interrupt threshold. This value is compared to the top 8 bits of the accelerometer 4g output.*

FFI_CNTL2 - Free Fall Control 2

This register has control settings for the free fall interrupt function.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
FFI_CNTL2	36h	R/W	00h	RST	FFICT<7>	FFICT<6>	FFICT<5>	FFICT<4>	FFICT<3>	FFICT<2>	FFICT<1>	FFICT<0>

FFICT<7:0> *- Accelerometer free fall interrupt counter. Every count is calculated as 1/ODR delay period.*

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FFI_CNTL3 - Free Fall Control 3

This register has control settings for the free fall interrupt function.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
FFI_CNTL3	37h	R/W	00h	RST	FFI_EN	FFIUL	SPARE_0037<5>	SPARE_0037<4>	DCRM	OFFI<2>	OFFI<1>	OFFI<0>

FFI_EN *- Accelerometer freefall engine enable*
FFI_EN = 0 – disabled
FFI_EN = 1 – enabled

FFIUL *- Accelerometer Freefall Interrupt latch/un-latch control for interrupt GPIO1/2*
FFIUL = 0 – latched
FFIUL = 1 – un-latched

DCRM – *Debounce methodology control.*
DCRM = 0 - count up/down
DCRM = 1- count up/reset.

OFFI<2:0> *- Output Data Rate at which the free fall detection performs its function.*

OFFI<2>	OFFI <1>	OFFI <0>	Output Data Rate (Hz)
0	0	0	12.5
0	0	1	25
0	1	0	50
0	1	1	100
1	0	0	200
1	0	1	400
1	1	0	800
1	1	1	1600

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ODCNTL - Output Data Control Register

Output data control register

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
ODCNTL	38h	R/W	22h	RST	OSM<3>	OSM<2>	OSM<1>	OSM<0>	OSA<3>	OSA<2>	OSA<1>	OSA<0>

OSA<3:0> - *Rate at which data samples from the accelerometer will be updated in the register map.*

OSA<3>	OSA<2>	OSA<1>	OSA<0>	Output Data Rate (Hz)
0	0	0	0	12.5**
0	0	0	1	25**
0	0	1	0	50**
0	0	1	1	100**
0	1	0	0	200**
0	1	0	1	400*
0	1	1	0	800
0	1	1	1	1600
1	0	0	0	0.781**
1	0	0	1	1.563**
1	0	1	0	3.125**
1	0	1	1	6.25**
1	1	0	0	25.6kHz, ST 0.8kHz
1	1	0	1	25.6kHz, ST 1.6kHz
1	1	1	0	25.6kHz, ST 3.2kHz
1	1	1	1	25.6kHz

Accelerometer Sampling Rate

OSM<3:0> *- Rate at which data samples from the magnetometer (and temperature sensor if enabled) will be updated in the register map.*

OSM<3>	OSM<2>	OSM<1>	OSM<0>	Output Data Rate (Hz)
0	0	0	0	12.5**
0	0	0	1	25**
0	0	1	0	50**
0	0	1	1	100**
0	1	0	0	200**
0	1	0	1	400*
0	1	1	0	800
0	1	1	1	1600
1	0	0	0	0.781**
1	0	0	1	1.563**
1	0	1	0	3.125**
1	0	1	1	6.25**
1	1	0	0	12.8kHz (polarity bit bypassed)
1	1	0	1	12.8kHz (polarity bit bypassed)
1	1	1	0	12.8kHz (polarity bit bypassed)
1	1	1	1	12.8kHz (polarity bit bypassed)

Magnetometer Sampling Rate

Note: The FIFO buffer will be updated at the faster of the two output data rates (OSM or OSA).
* RES<0,0> available, all others will default to full power mode.
** RES<0,0> and RES<0,1> available, all others will default to full power mode.

Before changing the ODR of a sensor, both sensors should be in stand-by. Write the new ODR value(s) to ODCNTL, and then enable the sensor(s).

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CNTL1 - Control Register 1

Control register that controls the main feature set.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
CNTL1	39h	R/W	00h	RST	SRST	STEN	STPOL	Reserved	COTC	Reserved	SPARE_0039<1>	SPARE_0039<0>

SRST *Software Reset function*

SRST = 0 – no action

SRST = 1 – start POR routine

STEN *- ST enable. This bit enables the self-test mode that will produce a change in both the accelerometer and magnetometer transducers and can be measured in the output registers.*

STEN = 0 – ST is disabled

STEN = 1 – ST is enabled.

STPOL *– Accelerometer and Magnetometer ST polarity.*

STPOL = 0 – ST polarity is positive

STPOL = 1 – ST polarity is negative.

COTC *enables the command test function*

COTC= 0 – no action

COTC = 1 – sets AAh to COTR register, when the COTR register is read, COTC is cleared and STR = 55h.

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CNTL2 - Control Register 2

This is used to enable and disable the sensors.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
CNTL2	3Ah	R/W	00h	RST	SPARE_003A<7>	TEMP_EN	Gsel<1>	Gsel<0>	RES<1>	RES<0>	MAG_EN	ACCEL_EN

TEMP_EN *controls the operating mode of the ASIC_AO's temperature sensors. MAG_EN must also be enabled for temperature data to be converted. Output data rate is locked to the magnetometer's OSM.*

Temp_EN = 0 – stand-by mode

Temp_EN = 1 – operating mode, magnetometer and temperature output registers are updated at the selected output data rate.

GSEL<1, 0> *selects the acceleration range of the accelerometer outputs per the following table.*

GSEL<1>	GSEL<0>	Range
0	0	+/-2g
0	1	+/-4g
1	0	+/-8g
1	1	+/-16g

Selected Acceleration Range

RES<1, 0> *selects the resolution of both sensors.*

RES<1>	RES<0>	Accelerometer over sample	Magnetometer over sample
0	0	4	2
0	1	32	16
1	0	maximum	maximum
1	1	maximum	maximum

Selected resolution range

MAG_EN *controls the operating mode of the ASIC_AO's magnetometer sensors.*

MAG_EN = 0 – stand-by mode.

MAG_EN = 1 – operating mode, magnetometer output registers are updated at the selected output data rate.

ACCEL_EN *controls the operating mode of the ASIC_AO's accelerometer*

ACCEL_EN = 0 – stand-by mode.

ACCEL_EN = 1 – operating mode, accelerometer output registers are updated at the selected output data rate.

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COTR - Command Test Response

This register can be used to verify proper communication functionality. It always has a byte value of 0x55h unless the COTC bit in CNTL1 is set. At that point this value is set to 0xAAh. The byte value is returned to 0x55h after reading this register.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
COTR	3Ch	R	55h		COTR<7>	COTR<6>	COTR<5>	COTR<4>	COTR<3>	COTR<2>	COTR<1>	COTR<0>

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BUF_CTRL_1,2,3

These registers control the buffer sample buffer operation.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
BUF_CTRL_1	77h	R/W	00h	RST	SMT_TH<7>	SMT_TH<6>	SMT_TH<5>	SMT_TH<4>	SMT_TH<3>	SMT_TH<2>	SMT_TH<1>	SMT_TH<0>
BUF_CTRL_2	78h	R/W	00h	RST	SPARE_0078<7>	SPARE_0078<6>	SPARE_0078<5>	SPARE_0078<4>	SPARE_0078<3>	BUF_M<1>	BUF_M<0>	SMT_TH<8>
BUF_CTRL_3	79h	R/W	00h	RST	BFI_EN	BUF_AX	BUF_AY	BUF_AZ	BUF_MX	BUF_MY	BUF_MZ	BUF_TEMP

SMP_TH<8,0> Sample Threshold *- determines the number of data bytes that will trigger a watermark interrupt or will be saved prior to a trigger event. The maximum number of data bytes is 384 (example - 32 samples of 3 axis of accel and 3 axis of mag by 2 bytes per axis).*

BUF_M1<1,0> *- selects the operating mode of the sample buffer*

BUF_M<1>	BUF_M<0>	Mode	Description	Sample Threshold Operation
0	0	FIFO	The buffer collects 384 bytes of data until full, collecting new data only when the buffer is not full.	Specifies how many buffer samples are needed to trigger a watermark interrupt.
0	1	Stream	The buffer holds the last 384 bytes of data. Once the buffer is full, the oldest data is discarded to make room for newer data.	Specifies how many buffer samples are needed to trigger a watermark interrupt.
1	0	Trigger	When a trigger event occurs (interrupt is caused by one of the digital engines or when a logic high signal occurs on the TRIG pin), the buffer holds the last data set of SMP_TH[8:0] samples before the trigger event and then continues to collect data until full. New data is collected only when the buffer is not full.	Specifies how many buffer samples before the trigger event are retained in the buffer.
1	1	FILO	The buffer holds the last 384 bytes of data. Once the buffer is full, the oldest data is discarded to make room for newer data. Reading from the buffer in this mode will return the most recent data first.	Specifies how many buffer samples are needed to trigger a watermark interrupt.

BFI_EN *controls the buffer full interrupt*
BUF_FIE = 0 – the buffer full interrupt, BFI is disabled
BUF_FIE = 1 – the buffer full interrupt, BFI will be triggered when the buffer is full

BUF_(AX, AY, AZ, MX, MY, MZ, TEMP) *controls the data to be buffered.*
BUF_(AX, AY,AZ, MX, MY, MZ, TEMP) = 0 – indicated data is not buffered
BUF_(AX, AY,AZ, MX, MY, MZ, TEMP)= 1 – indicated data is buffered

BUF_CLEAR

Latched buffer status information and the entire sample buffer are cleared when any data is written to this register.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
BUF_CLEAR	7Ah	W		OTF	BUFCLR<7>	BUFCLR<6>	BUFCLR<5>	BUFCLR<4>	BUFCLR<3>	BUFCLR<2>	BUFCLR<1>	BUFCLR<0>

BUF_STATUS_1,2,3

This register reports the status of the sample buffer.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
BUF_STATUS_1	7Bh	R	00h		SMP_LEV<7>	SMP_LEV<6>	SMP_LEV<5>	SMP_LEV<4>	SMP_LEV<3>	SMP_LEV<2>	SMP_LEV<1>	SMP_LEV<0>
BUF_STATUS_2	7Ch	R	00h		SMP_PAST<5>	SMP_PAST<4>	SMP_PAST<3>	SMP_PAST<2>	SMP_PAST<1>	SMP_PAST<0>	BUF_TRIG	SMP_LEV<8>
BUF_STATUS_3	7Dh	R	00h		SMP_PAST<13>	SMP_PAST<12>	SMP_PAST<11>	SMP_PAST<10>	SMP_PAST<9>	SMP_PAST<8>	SMP_PAST<7>	SMP_PAST<6>

SMP_LEV<8:0> Sample Level*; reports the number of data bytes that have been stored in the sample buffer. If this register reads 0, no data has been stored in the buffer. If the buffer data is read past this level the part will return 32,767 (maximum value).*

Buffered Outputs	*Maximum sets*	*Maximum bytes*
1	*192*	*384*
2	*96*	*384*
3	*64*	*384*
4	*48*	*384*
5	*38*	*380*
6	*32*	*384*
7	*27*	*378*

BUF_TRIG *reports the status of the buffer's trigger function if this mode has been selected. When using trigger mode, a buffer read should only be performed after a trigger event.*

SMP_PAST<8:0> Sample over flow*; reports the number of data bytes that have been missed since the sample buffer was filled. If this register reads 0, the buffer has not over flowed. This is cleared for "BUF_CLEAR" command and when the data is read from "BUF_READ"*

BUF_READ

Data in the buffer can be read according to the BUF_M settings in BUF_CTRL2 by executing this command. More samples can be retrieved by continuing to toggle SCL after the read command is executed. Data should be read using auto-increment. Additional samples cannot be written to the buffer while data is being read from the buffer using auto-increment mode. Output data is in 2's Complement format.

Register	*Addr*	*R/W*	*POR*	*Wrt*	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit3*	*Bit 2*	*Bit 1*	*Bit 0*
BUF_READ	7Eh	R			BUF<7>	BUF<6>	BUF<5>	BUF<4>	BUF<3>	BUF<2>	BUF<1>	BUF<0>

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Sample Buffer Feature Description

The sample buffer feature of the ASIC_AO accumulates and outputs data based on how it is configured. There are 4 buffer modes available. Data is collected at the highest ODR specified by OSA[3:0] and OSM[3:0] in the ODCNTL (Output Data Control) Register. Each buffer mode accumulates data, reports data, and interacts with status indicators in a slightly different way.

FIFO Mode

Data Accumulation

Sample collection stops when the buffer is full.

Data Reporting

Data is reported with the oldest byte of the oldest sample first (X_L or X based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or reading greater than SMPX.

$$SMPX = SMP\_LEV[8:0] - SMP\_TH[8:0]$$

Equation 1: Samples Above Sample Threshold

Stream Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 1).

Trigger Mode

Data Accumulation

When a physical interrupt is caused by one of the digital engines or when a logic high signal occurs on the TRIG pin, the trigger event is asserted and SMP_TH[8:0] samples prior to the event are retained. Sample collection continues until the buffer is full.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

When a physical interrupt occurs and there are at least SMP_TH[8:0] samples in the buffer, BUF_TRIG in BUF_STATUS_REG2 is asserted.

FILO Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the newest byte of the newest sample first (Z_H or Z based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 1).

Buffer Operation

The following diagrams illustrate the operation of the buffer conceptually. Actual physical implementation has been abstracted to offer a simplified explanation of how the different buffer modes operate. Regardless of the selected mode, the buffer fills sequentially, two-byte at a time and one set_count number of bytes at the highest ODR. Figure 7 shows one 14-byte data sample with all devices (accelerometer, temp sensor and magnetometer) enabled. Note the location of the FILO read pointer versus that of the FIFO read pointer. Figure 8 shows one 12-byte data sample with accelerometer and magnetometer enabled and temperature sensor disabled. Figure 8 - Figure 17 represent a 10-sample version of the buffer (for simplicity), with Sample Threshold set to 8.

Note: When the BUF_CLEAR command is asserted, the buffer read pointer is moved to the location of the buffer write pointer.

Note: If the buffer control states that a particular sensor's data should be buffered, but that sensor is not enabled, then all buffer entries for that sensor will be that sensor's last ADC conversion prior to it being disabled.

Index	Byte	
0	ACCEL X_L	<---- FIFO read pointer
1	ACCEL X_H	
2	ACCEL Y_L	
3	ACCEL Y_H	
4	ACCEL Z_L	
5	ACCEL Z_H	
6	MAG X_L	
7	MAG X_H	
8	MAG Y_L	
9	MAG Y_H	
10	MAG Z_L	
11	MAG Z_H	
12	TEMP_L	
13	TEMP_H	<---- FILO read pointer
14		buffer write pointer (Sample Level) ---->

Figure 7. One Buffer Sample with accelerometer, temperature sensor and magnetometer all enabled

Index	Byte	
0	ACCEL X_L	<---- FIFO read pointer
1	ACCEL X_H	
2	ACCEL Y_L	
3	ACCEL Y_H	
4	ACCEL Z_L	
5	ACCEL Z_H	
6	MAG X_L	
7	MAG X_H	
8	MAG Y_L	
9	MAG Y_H	
10	MAG Z_L	
11	MAG Z_H	<---- FILO read pointer
12		buffer write pointer (Sample Level) ---->

Figure 8. One Buffer Sample with accelerometer and magnetometer enabled and temperature sensor disabled

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Note in Figure 9 the location of the FILO read pointer versus that of the FIFO read pointer. The buffer write pointer shows where the next sample will be written to the buffer.

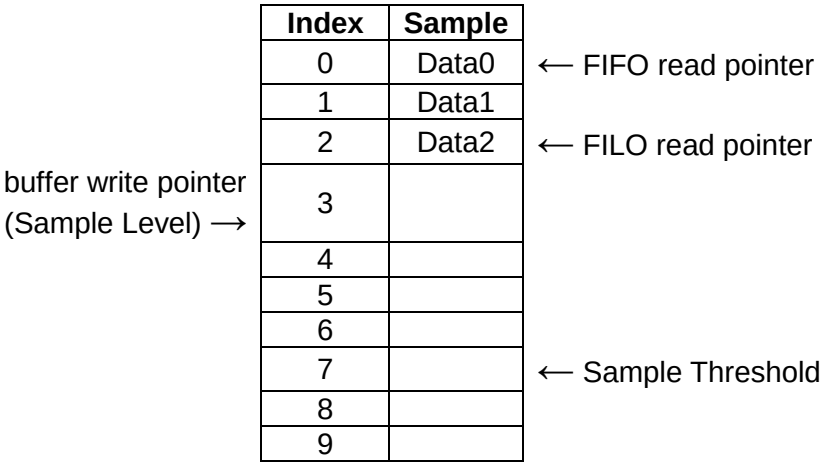

Figure 9. Buffer Filling

The buffer continues to fill sequentially until the Sample Threshold is reached. Note in Figure 10 the location of the FILO read pointer versus that of the FIFO read pointer.

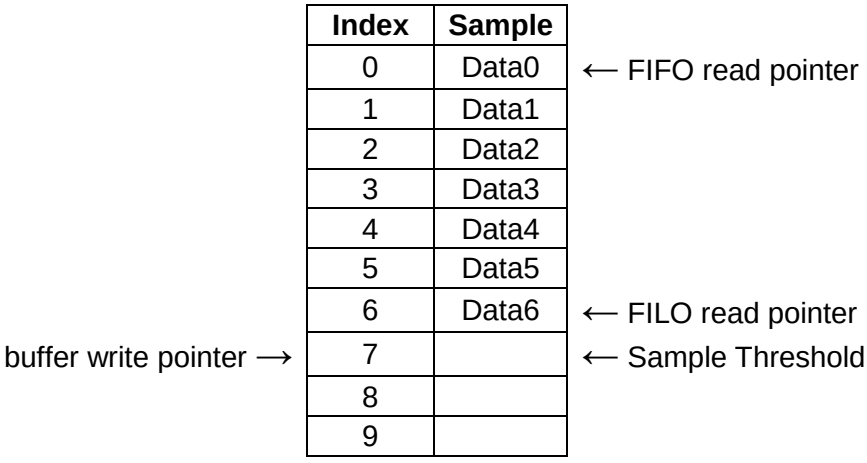

Figure 10. Buffer Approaching Sample Threshold

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In FIFO, Stream, and FILO modes, a watermark interrupt is issued when the number of samples in the buffer reaches the Sample Threshold. In trigger mode, this is the point where the oldest data in the buffer is discarded to make room for newer data.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	
	7	Data7	← Sample Threshold/FILO read pointer
buffer write pointer →	8		
	9		

Figure 11. Buffer at Sample Threshold

In trigger mode, data is accumulated in the buffer sequentially until the Sample Threshold is reached. Once the Sample Threshold is reached, the oldest samples are discarded when new samples are collected. Note in Figure 12 how Data0 was thrown out to make room for Data8.

	Index	Sample	
	0	Data1	← Trigger read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
Trigger write pointer →	7	Data8	← Sample Threshold
	8		
	9		

Figure 12. Additional Data Prior to Trigger Event

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After a trigger event occurs, the buffer no longer discards the oldest samples, and instead begins accumulating samples sequentially until full. The buffer then stops collecting samples, as seen in Figure 13. This results in the buffer holding SMP_TH[8:0] samples prior to the trigger event, and SMPX samples after the trigger event.

Index	Sample	
0	Data1	← Trigger read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	

Figure 13. Additional Data After Trigger Event

In FIFO, Stream, FILO, and Trigger (after a trigger event has occurred) modes, the buffer continues filling sequentially after the Sample Threshold is reached. Sample accumulation after the buffer is full depends on the selected operation mode. FIFO and Trigger modes stop accumulating samples when the buffer is full, and Stream and FILO modes begin discarding the oldest data when new samples are accumulated.

Index	Sample	
0	Data0	← FIFO read pointer
1	Data1	
2	Data2	
3	Data3	
4	Data4	
5	Data5	
6	Data6	
7	Data7	← Sample Threshold
8	Data8	
9	Data9	← FILO read pointer

Figure 14. Buffer Full

After the buffer has been filled in FILO or Stream mode, the oldest samples are discarded when new samples are collected. Note in Figure 15 how Data0 was thrown out to make room for Data10.

Index	Sample	
0	Data1	← FIFO read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	← FILO read pointer

Figure 15. Buffer Full – Additional Sample Accumulation in Stream or FILO Mode

In FIFO, Stream, or Trigger mode, reading one sample from the buffer will remove the oldest sample and effectively shift the entire buffer contents up, as seen in Figure 16.

	Index	Sample	
	0	Data1	← FIFO read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
	7	Data8	← Sample Threshold
	8	Data9	← FILO read pointer
buffer write pointer →	9		

Figure 16. FIFO Read from Full Buffer

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In FILO mode, reading one sample from the buffer will remove the newest sample and leave the older samples untouched, as seen in Figure 17.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	
	7	Data7	← Sample Threshold
	8	Data8	← FILO read pointer
buffer write pointer →	9		

Figure 17. FILO Read from Full Buffer

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Revision History

REVISION	DESCRIPTION	DATE
1.0	Initial Release	29 May 2015
2.0	Updated Writing/Reading Description in I2C Updated current consumption diagrams Updated pin description table Added Notice Revised environmental spec (RoHS + REACH)	20 Oct 2015
3.0	Updated *Figure 6. Temperature (°C) Calculation* 256counts/C for 16bit. Updated Trigger Buffer Description	01 Mar 2016

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