

IGBT SIP Module (Fast IGBT)



IMS-2

PRODUCT SUMMARY	
OUTPUT CURRENT IN A TYPICAL 5.0 kHz MOTOR DRIVE	
V_{CES}	600 V
I_{RMS} per phase (3.1 kW total) with $T_C = 90\text{ }^\circ\text{C}$	11 A
T_J	125 $^\circ\text{C}$
Supply voltage	360 V_{DC}
Power factor	0.8
Modulation depth See fig. 1	115 %
$V_{CE(on)}$ (typical) at $I_C = 4.8\text{ A}$, 25 $^\circ\text{C}$	1.41 V
Speed	1 kHz to 8 kHz
Package	SIP
Circuit	Three phase inverter

FEATURES

- Fully isolated printed circuit board mount package
- Switching-loss rating includes all “tail” losses
- HEXFRED® soft ultrafast diodes
- Optimized for medium speed, see fig. 1 for current vs. frequency curve
- Designed and qualified for industrial level
- UL approved file E78996
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

DESCRIPTION

The IGBT technology is the key to the advanced line of IMS (Insulated Metal Substrate) power modules. These modules are more efficient than comparable bipolar transistor modules, while at the same time having the simpler gate-drive requirements of the familiar power MOSFET. This superior technology has now been coupled to a state of the art materials system that maximizes power throughput with low thermal resistance. This package is highly suited to motor drive applications and where space is at a premium.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Collector to emitter voltage	V_{CES}		600	V
Continuous collector current, each IGBT	I_C	$T_C = 25\text{ }^\circ\text{C}$	8.8	A
		$T_C = 100\text{ }^\circ\text{C}$	4.8	
Pulsed collector current	I_{CM}	Repetitive rating; $V_{GE} = 20\text{ V}$, pulse width limited by maximum junction temperature. See fig. 20	26	
Clamped inductive load current	I_{LM}	$V_{CC} = 80\%$ (V_{CES}), $V_{GE} = 20\text{ V}$, $L = 10\text{ }\mu\text{H}$, $R_G = 50\text{ }\Omega$ See fig. 19	800	
Diode continuous forward current	I_F	$T_C = 100\text{ }^\circ\text{C}$	3.4	
Diode maximum forward current	I_{FM}		26	
Gate to emitter voltage	V_{GE}		± 20	V
Isolation voltage	V_{ISOL}	Any terminal to case, $t = 1\text{ min}$	2500	V_{RMS}
Maximum power dissipation, each IGBT	P_D	$T_C = 25\text{ }^\circ\text{C}$	23	W
		$T_C = 100\text{ }^\circ\text{C}$	9.1	
Operating junction and storage temperature range	T_J, T_{Stg}		-40 to +150	$^\circ\text{C}$
Soldering temperature		For 10 s	300 (0.063" (1.6 mm) from case)	
Mounting torque		6-32 or M3 screw	5 to 7 (0.55 to 0.8)	lbf · in (N · m)

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TYP.	MAX.	UNITS
Junction to case, each IGBT, one IGBT in conduction	R_{thJC} (IGBT)	-	5.5	$^\circ\text{C/W}$
Junction to case, each diode, one diode in conduction	R_{thJC} (diode)	-	9.0	
Case to sink, flat, greased surface	R_{thCS} (module)	0.1	-	
Weight of module		20 (0.7)	-	g (oz.)



ELECTRICAL SPECIFICATIONS (T _J = 25 °C unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Collector to emitter breakdown voltage	V _{(BR)CES}	V _{GE} = 0 V, I _C = 250 μA Pulse width ≤ 80 μs, duty factor ≤ 0.1 %	600	-	-	V
Temperature coeff. of breakdown voltage	ΔV _{(BR)CES} /ΔT _J	V _{GE} = 0 V, I _C = 1.0 mA	-	0.72	-	V/°C
Collector to emitter saturation voltage	V _{CE(on)}	I _C = 4.8 A	-	1.41	1.7	V
		I _C = 8.8 A	-	1.66	-	
		I _C = 4.8 A, T _J = 150 °C	-	1.42	-	
Gate threshold voltage	V _{GE(th)}	V _{CE} = V _{GE} , I _C = 250 μA	3.0	-	6.0	
Gate to emitter leakage current	I _{GES}	V _{GE} = ± 20 V	-	-	± 100	nA
Temperature coeff. of threshold voltage	ΔV _{GE(th)} /ΔT _J	V _{GE} = 0 V, I _C = 1.0 mA	-	-11	-	mV/°C
Forward transconductance	g _{fe}	V _{CE} = 100 V, I _C = 4.8 A Pulse width 5.0 μs; single shot	2.9	5.0	-	S
Zero gate voltage collector current	I _{CES}	V _{GE} = 0 V, V _{CE} = 600 V	-	-	250	μA
		V _{GE} = 0 V, V _{CE} = 600 V, T _J = 150 °C	-	-	1700	
Diode forward voltage drop	V _{FM}	I _C = 8.0 A	-	1.4	1.7	V
		I _C = 8.0 A, T _J = 150 °C	See fig. 13	-	1.3	

SWITCHING CHARACTERISTICS (T _J = 25 °C unless otherwise specified)								
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS		
Total gate charge (turn on)	Q _g	I _C = 4.8 A V _{CC} = 400 V See fig. 8	-	30	45	nC		
Gate to emitter charge (turn on)	Q _{ge}		-	4.0	6.0			
Gate to collector charge	Q _{gc}		-	13	20			
Turn-on delay time	t _{d(on)}	T _J = 25 °C I _C = 4.8 A, V _{CC} = 480 V V _{GE} = 15 V, R _G = 50 Ω Energy losses include "tail" and diode reverse recovery. See fig. 9, 10, 18	-	49	-	ns		
Rise time	t _r		-	22	-			
Turn-off delay time	t _{d(off)}		-	200	300			
Fall time	t _f		-	214	320			
Turn-on switching loss	E _{on}		-	0.23	-		mJ	
Turn-off switching loss	E _{off}		-	0.33	-			
Total switching loss	E _{ts}	-	0.45	0.70				
Turn-on delay time	t _{d(on)}	T _J = 150 °C, I _C = 4.8 A, V _{CC} = 480 V V _{GE} = 15 V, R _G = 50 Ω Energy losses include "tail" and diode reverse recovery See fig. 10, 11, 18	-	48	-	ns		
Rise time	t _r		-	25	-			
Turn-off delay time	t _{d(off)}		-	435	-			
Fall time	t _f		-	364	-			
Total switching loss	E _{ts}		-	0.93	-		mJ	
Input capacitance	C _{ies}		V _{GE} = 0 V V _{CC} = 30 V	-	340		-	pF
Output capacitance	C _{oes}	See fig. 7		-	63	-		
Reverse transfer capacitance	C _{res}	-		5.9	-			
Diode reverse recovery time	t _{rr}	T _J = 25 °C	See fig. 14	-	37	55	ns	
		T _J = 125 °C		-	55	90		
Diode peak reverse recovery current	I _{rr}	T _J = 25 °C	See fig. 15	-	3.5	50	A	
		T _J = 125 °C		-	4.5	8.0		
Diode reverse recovery charge	Q _{rr}	T _J = 25 °C	See fig. 16	I _F = 8.0 A V _R = 200 V dl/dt = 200 A/μs	-	65	138	nC
		T _J = 125 °C			-	124	360	
Diode peak rate of fall of recovery during t _b	dl _{(rec)M} /dt	T _J = 25 °C	See fig. 17	-	240	-	A/μs	
		T _J = 125 °C		-	210	-		

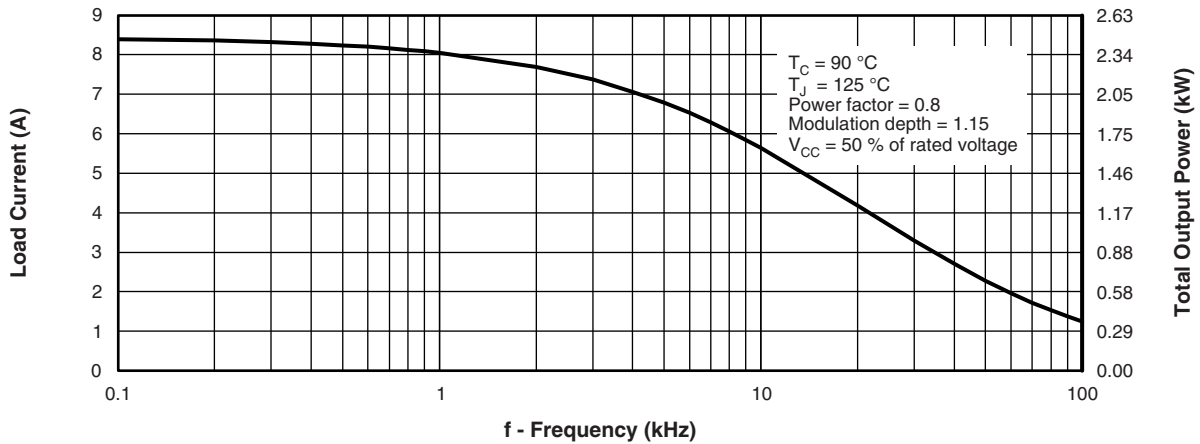


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of Fundamental)

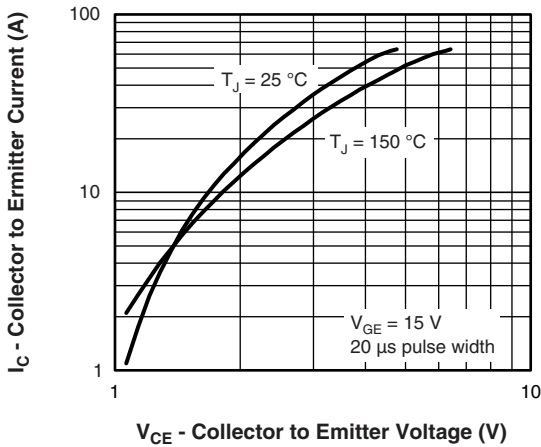


Fig. 2 - Typical Output Characteristics

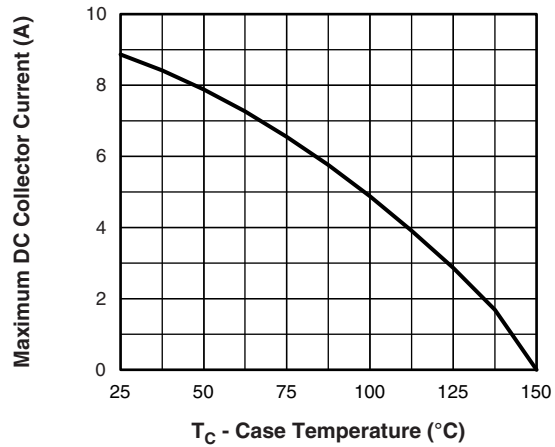


Fig. 4 - Maximum Collector Current vs. Case Temperature

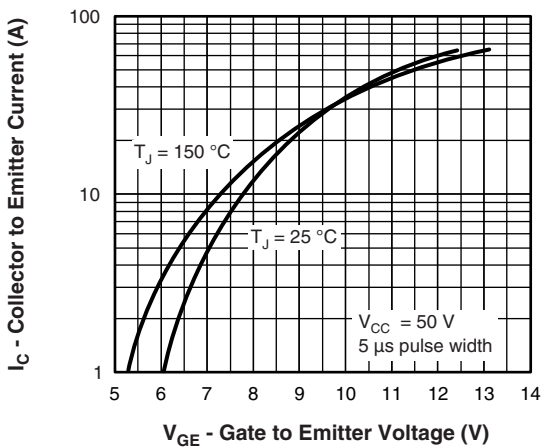


Fig. 3 - Typical Transfer Characteristics

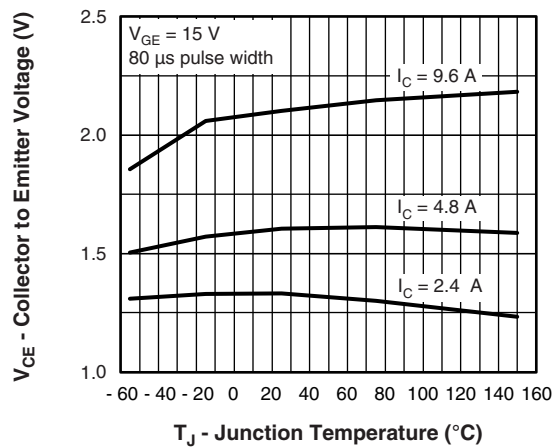


Fig. 5 - Typical Collector to Emitter Voltage vs. Junction Temperature

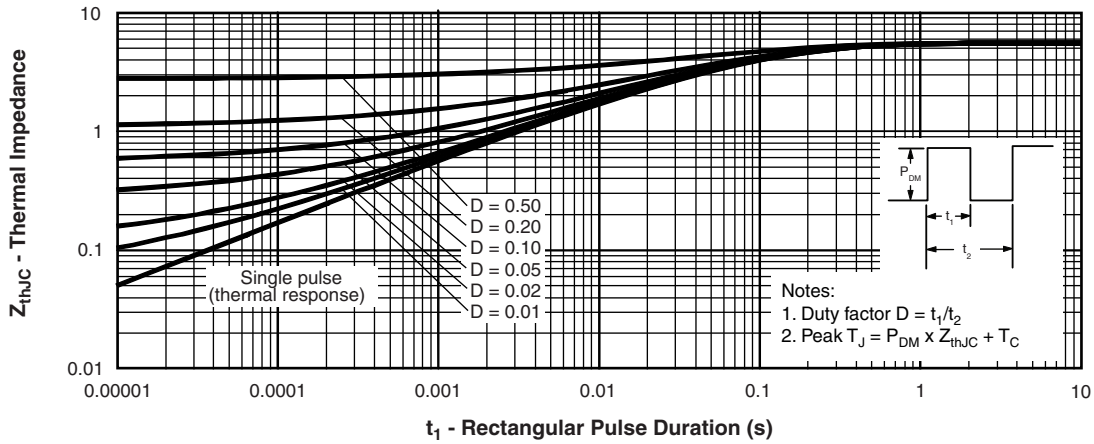


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction to Case

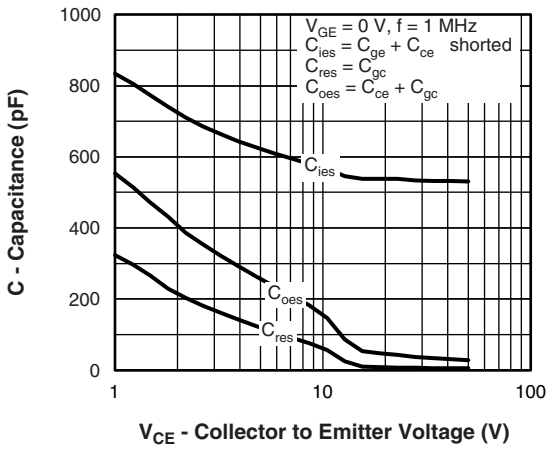


Fig. 7 - Typical Capacitance vs. Collector to Emitter Voltage

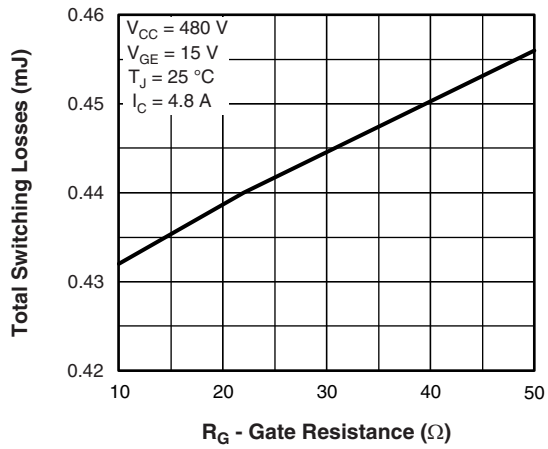


Fig. 9 - Typical Switching Losses vs. Gate Resistance

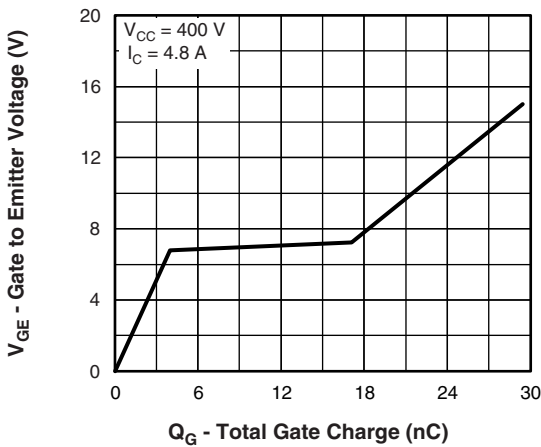


Fig. 8 - Typical Gate Charge vs. Gate to Emitter Voltage

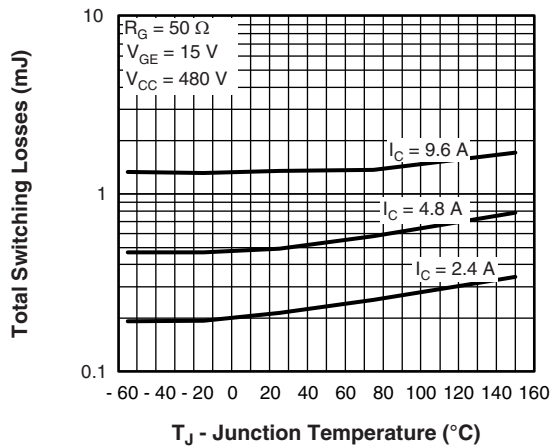


Fig. 10 - Typical Switching Losses vs. Junction Temperature

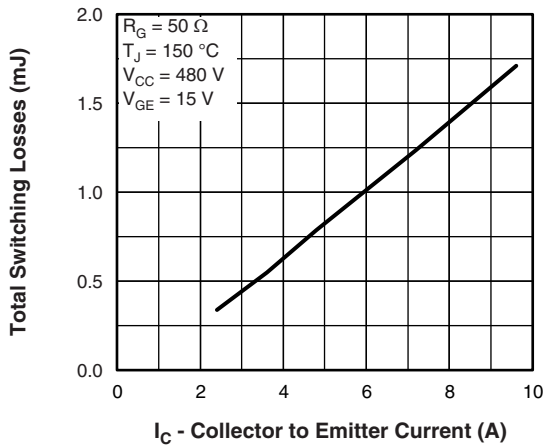


Fig. 11 - Typical Switching Losses vs. Collector to Emitter Current

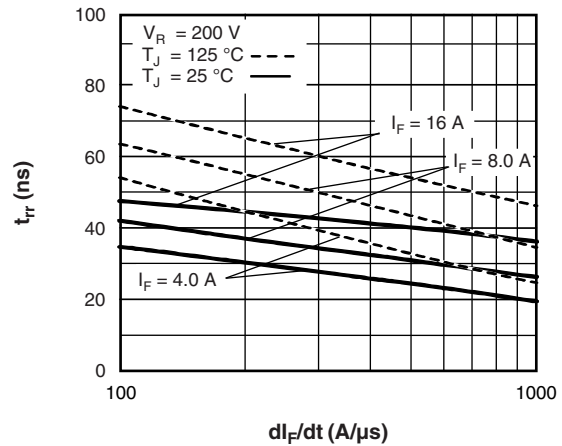


Fig. 14 - Typical Reverse Recovery Time vs. dI_F/dt

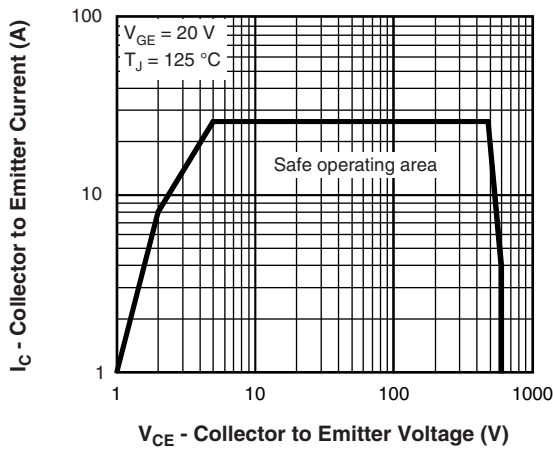


Fig. 12 - Turn-Off SOA

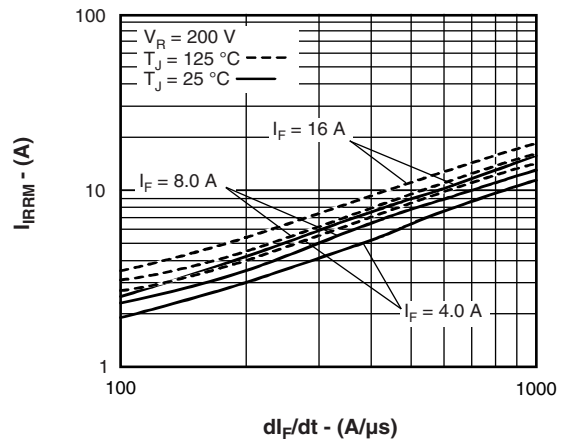


Fig. 15 - Typical Recovery Current vs. dI_F/dt

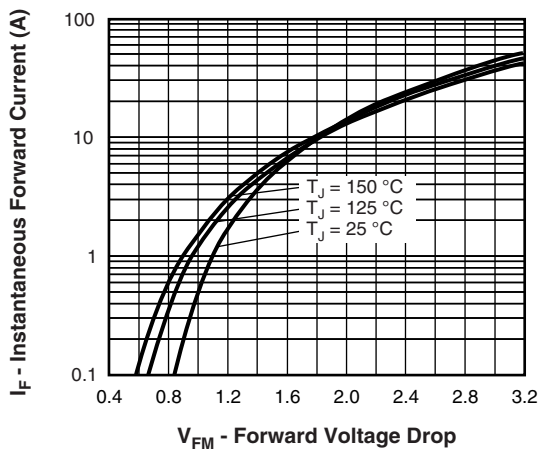


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

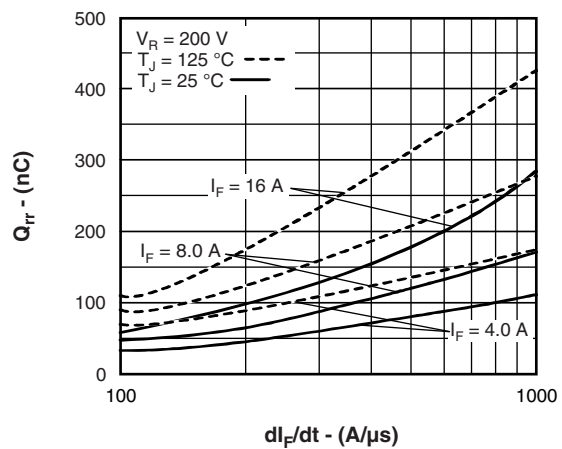


Fig. 16 - Typical Stored Charge vs. dI_F/dt

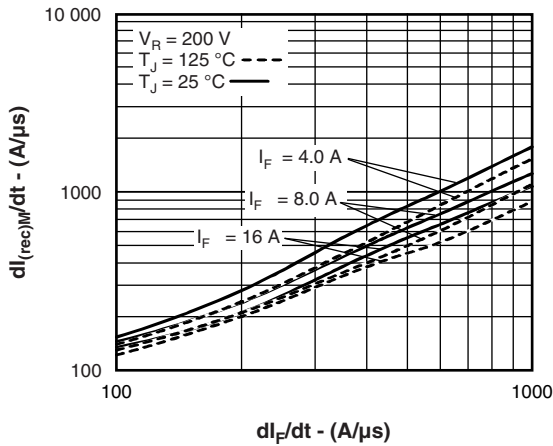


Fig. 17 - Typical $dI_{(REC)M}/dt$ vs dI_F/dt

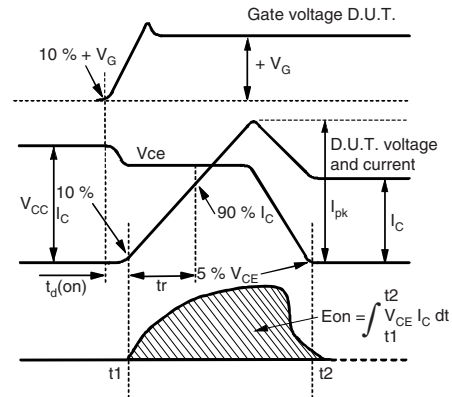


Fig. 18c - Test Waveforms of Circuit of Fig. 18a, Defining E_{on} , $t_{d(on)}$, t_r

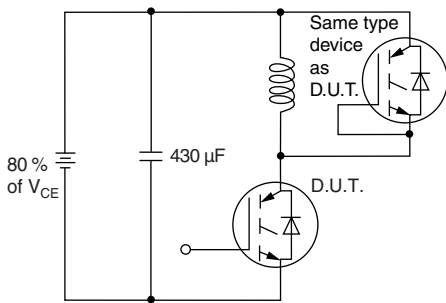


Fig. 18a - Test Circuit for Measurement of I_{LM} , E_{on} , $E_{off(diode)}$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

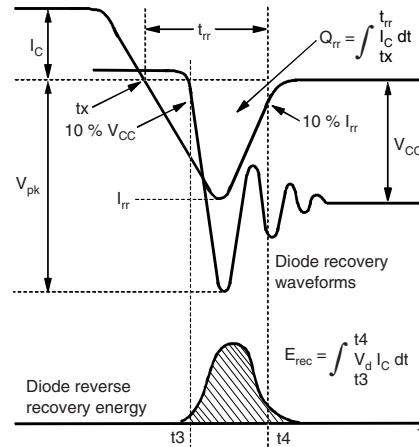


Fig. 18d - Test Waveforms of Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

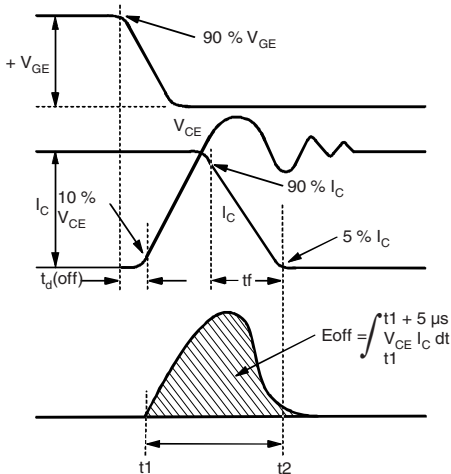


Fig. 18b - Test Waveforms of Circuit of Fig. 18a, Defining E_{off} , $t_{d(off)}$, t_f

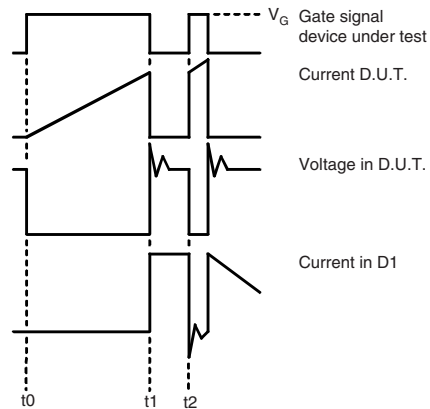


Fig. 18e - Macro Waveforms for Figure 18a's Test Circuit

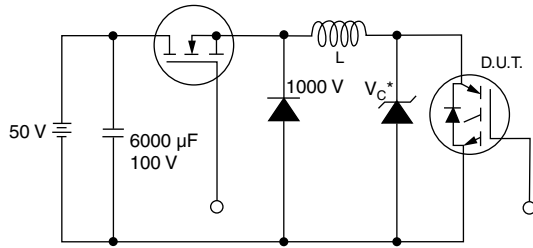


Fig. 19 - Clamped Inductive Load Test Circuit

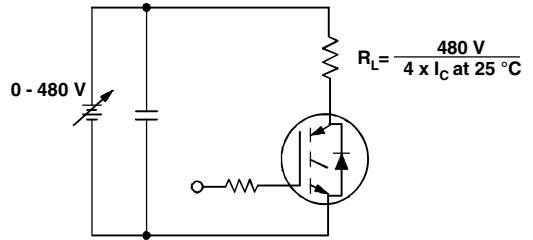
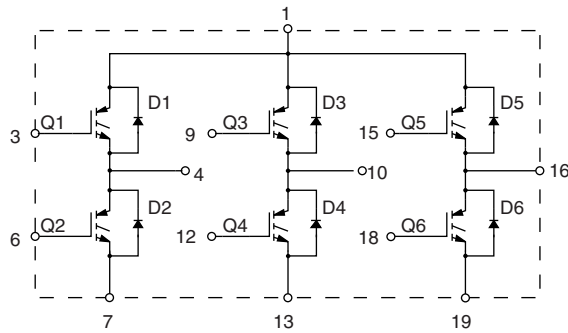


Fig. 20 - Pulsed Collector Current Test Circuit

CIRCUIT CONFIGURATION

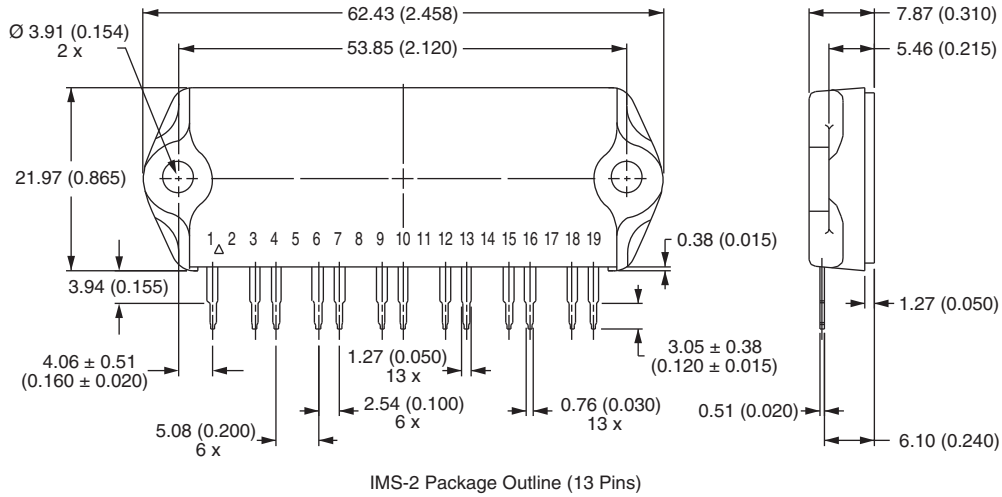


LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?95066
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IMS-2 (SIP)

DIMENSIONS in millimeters (inches)



Notes

- (1) Tolerance unless otherwise specified ± 0.254 mm (0.010")
- (2) Controlling dimension: inch
- (3) Terminal numbers are shown for reference only



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